NSI6602B-DSWR

High Reliability Isolated Dual-Channel Gate Driver

Description

NSI6602B-DSWR is a family of high reliability isolated dual channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. Each output could source 4A and sink 6A peak current with fast 25ns propagation delay and 5ns maximum delay matching.

The NSI6602B-DSWR provides 5000Vrms isolation in SOW-16 package. System robustness is supported by 150kV/us typical common-mode transient immunity(CMTI).

The driver operates with a maximum supply voltage of 30V, while the input-side accepts from 2.7V to 5V supplyvoltage. Under voltage lock-out (UVLO) protection issupported by all the power supply voltage pins.

Pin 1

SOW-16

Safety Regulatory Approvals

- UL recognition(Planned):
  5000Vrms for 1 minute per UL1577
- DIN EN IEC 60747-17(VDE 0884-17):2021-10
- CSA component notice 5A

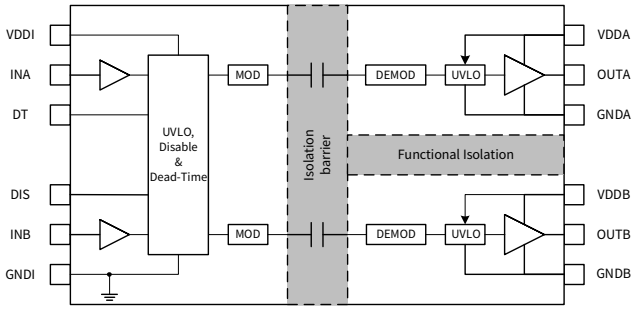
Applications

- MOSFET,IGBT,SiC and GaN gate driver
- Isolated DC-DC and AC-to-DC power supplies in server,telecom,and industry
- Motor drives and EV charging
- UPS and battery chargers
- DC-to-AC solar inverters

Features

- Isolated dual channel driver
- Input side supply voltage: 2.7V to 5.5V
- Driver side supply voltage: up to 30V with UVLO
- 4A peak source and 6A peak sink output
- High CMTI: ±200kV/us typical
- 25ns typical propagation delay
- 5ns maximum delay matching
- 6ns maximum pulse width distortion
- Programmable deadtime
- Accepts minimum input pulse width 20ns
- Operation temperature:-40°C~105°C
- RoHS & REACH Qualified

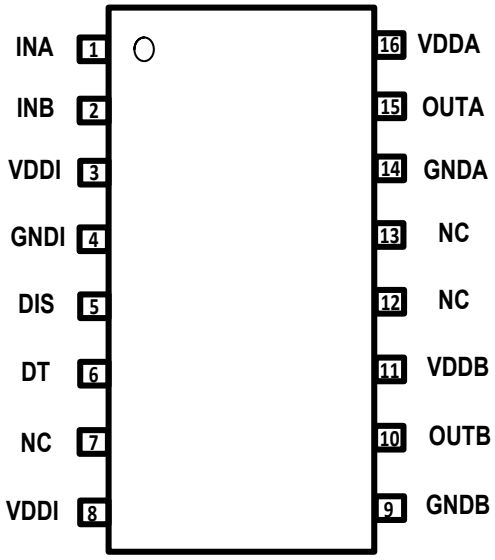
Functional Block Diagram



Product Family

Part Number	Peak Current	UVLO	DT	DIS	Package
NSI6602B-DSWR	+4.0A/-6.0A	8.5V/8.0V	Y	Y	SOW-16

Pin Configuration



SOW-16

Pin Description

No.	Symbol	Description
1	INA	TTL/CMOS compatible input signal for channel A with internal pull down to GND.
2	INB	TTL/CMOS compatible input signal for channel B with internal pull down to GND.
3,8	VDDI	Input side supply voltage.
4	GND	Input side ground reference.
5	DISABLE	Disable the isolator inputs and driver outputs if asserted high, enable if asserted low or left open
6	DT	Programmable deadtime control.
9	GNDB	Ground for output channel B
10	OUTB	Output gate driver for channel B
11	VDDB	Supply voltage for channel B
14	GNDA	Ground for output channel A
15	OUTA	Output gate driver for channel A
16	VDDA	Supply voltage for channel A
7,12,13	NC	Not connected

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Input Side Supply Voltage	VDDI to GNDI	-0.3	6	V
Input Signal Voltage	V_{IA}, V_{IB}, V_{DIS}	-0.3	6	
Output Side Supply Voltage	VDDA to GNDA, VDDB to GNDB	-0.3	30	
Channel A to Channel B Isolation Voltage	V_{ISOAB}	-	1500	
Electrostatic discharge	HBM	-4000	4000	
	CDM	-1500	1500	
Storage Temperature	T_S	-65	+150	°C
Junction Temperature	T_j	-40	+150	°C

Note : V_{DDI}, V_{IA}, V_{IB}, V_{DIS} are reference to G_{NDI}; V_{DDA}, V_{OUTA} is referenced to G_{NDA}; V_{DDB}, V_{OUTB} is referenced to G_{NDB}.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Input Side Supply Voltage	V_{DDI} to G_{NDI}	3.0	5.5	V
Input Signal Voltage	V_{IA}, V_{IB}, V_{DIS}	3.0	5.5	
Output Supply Voltage	V_{DDA} to G_{NDA}, V_{DDB} to G_{NDB}	7	20	
Input Signal Voltage	I_{NA},I_{NB},D_{IS},D_T	0	V_{VDDI}	
Junction Temperature	T_j	-40	150	
Operating Temperature	T_A	-40	125	°C

Note:Operation beyond recommended operating conditions may cause long term reliability issue or even damage to the IC.

Electrical Characteristics (DC)

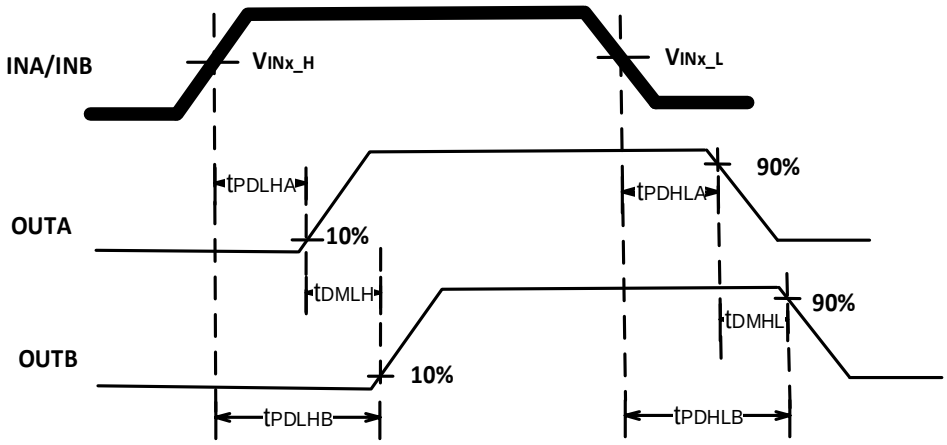
VDDI=3.3V or 5V, VDDA=VDDB=12V for H8233A/B, VDDA=VDDB=15V for H8233C, T_a=-40~125℃. Unless otherwise noted, typical values are tested at T_a=25℃.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Current leakage characteristics						
VDDI Quiescent Current	I_{VDDIQ}	-	0.4	2	mA	INA=0, INB=0
VDDI Operating Current	I_{VDDI}	-	11		mA	Input frequency 500kHz
VDDA/B Quiescent Current, per Channel	I_{VDDAQ}, I_{VDDBQ}	-	1.5	2.5	mA	INA=0,INB=0, VDDx=12V for 6V, 8V UVLO; VDDx=15V for 13V UVLO
VDDA/B Operation Current, per Channel	I_{VDDA}, I_{VDDB}	-	2.6	-	mA	100pF, 500KHz, VDDx=12V for 6V, 8V UVLO; VDDx=15V for 13V UVLO
UVLO						
VDDI UVLO Rising Threshold	V_{VDDI_ON}	2.35	2.55	2.75	V	
VDDI UVLO Falling Threshold	V_{VDDI_OFF}	2.15	2.35	2.55		
VDDI UVLO Hysteresis	V_{VDDI_HYS}	-	0.2	-		
VDDA/B UVLO Rising Threshold	V_{VDDO_ON}	7.5	8.0	8.5		
VDDA/B UVLO Falling Threshold	V_{VDDO_OFF}	7.0	7.5	8.0		
VDDA/B UVLO Hysteresis	V_{VDDO_HYS}	-	0.5	-		
Input Side Characteristic						
Input Pin Pull Down Resistance, INA, INB	R_{INA_PD}, R_{INB_PD},	-	100	-	kΩ	
Input Pin Pull Down Resistance, DIS(EN)	R_{DIS_PD}	-	100	-	kΩ	
Logic High Input Threshold	V_{INA_H}, V_{INB_H}, V_{DIS_H}	-	1.45	2	V	
Logic Low Input Threshold	V_{INA_L}, V_{INB_L}, V_{DIS_L}	0.8	1.3	-		
Input Hysteresis	V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}	-	0.15	-		
Output Side Characteristic						
Logic High Output Voltage	V_{VDDA}-V_{OUTA_H}, V_{VDDB}-V_{OUTB_H},	-	0.34	-	V	I_{out}=100mA
Logic Low Output Voltage	V_{OUTA_L}, V_{OUTB_L}	-	55	-	mV	I_{out}=100mA
Output Source Resistance	R_{OUTA_H}, R_{OUTB_H}	-	3.4	-	Ω	I_{out}=100mA
Output Sink Resistance	R_{OUTA_L}, R_{OUTB_L}	-	0.55	-	Ω	I_{out}=100mA
Peak Output Source Current	I_{OUTA+}, I_{OUTB+}	-	+4.0	-	A	VDDx=15V
Peak Output Sink Current	I_{OUTA-}, I_{OUTB-}	-	-6.0	-	A	VDDx=15V

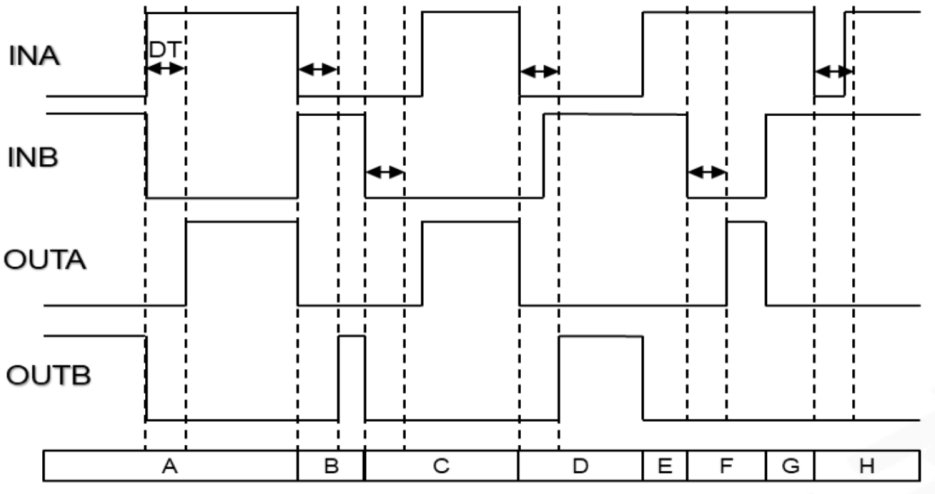
Switching Characteristics (AC)

VDDI=3.3V or 5V, VDDA=VDDB=12V for H8233A/B, VDDA=VDDB=15V for H8233C, Ta=25℃.

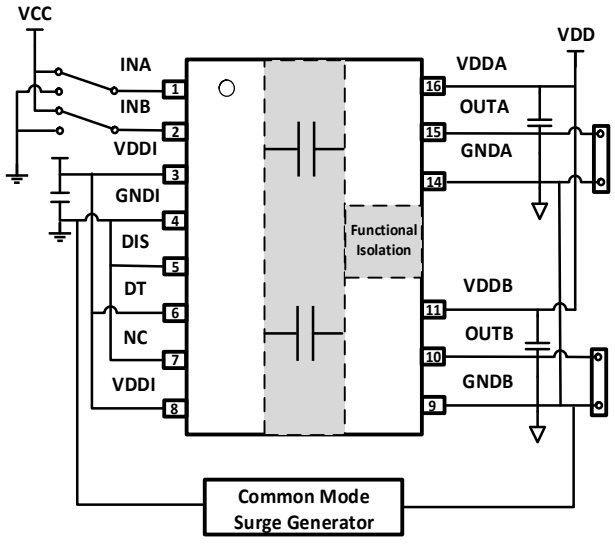
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Turn On Propagation Delay Time	t_{PDLH}	10	25	35	ns	$C_{OUTA/B}$=1 nF
Turn Off Propagation Delay Time	t_{PDHL}	10	25	35		$C_{OUTA/B}$=1 nF
Output Rise Time (20% to 80%)	t_R	-	7	16		$C_{OUTA/B}$=1.8nF, verified by design
Output Fall Time (90% to 10%)	t_F	-	6	12		$C_{OUTA/B}$=1.8nF, verified by design
Minimum Pulse Width	t_{PWmin}	-	10	15		$C_{OUTA/B}$=0 pF
Pulse Width Distortion $\lvert t_{PDHL}- t_{PDLH}\rvert$	t_{PWD}	-	-	6		
Channel to Channel Delay Matching	t_{DMLH}, t_{DMHL}	-	-	5		
Programmed Deadtime	t_{DT}	160	200	240		t_{DT}(ns)=10*R(KΩ); Test for R=20KΩ
Shutdown Time from Disable True	t_{DIS}	-	-	40		
Recovery Time from Disable False	T_{EN}	-	-	40		
VDDI Power-up Time Delay (Time from VDDI=VDDI_ON to OUTA/B=INA/B)	t_{start_VDDI}	-	8.5	15	us	INA or INB tied to VDDI
VDDA/B Power-up Time Delay (Time from VDDA/B=2V to OUTA/B=INA/B)	t_{start_VDDA}, t_{start_VDDB}	-	18	30	us	INA or INB tied to VDDI $C_{OUTA/B}$=1.8nF
High Level Common Mode Transient Immunity	$CMTI_H$	100	150	-	kV/us	
Low Level Common Mode Transient Immunity	$CMTI_L$	100	150	-	kV/us	



Propagation Delay and Delay Match Time



Input and Output Logic with Programmed Deadtime



CMTI Test Circuit

Feature Description

NSI6602B-DSWR is a flexible dual channel isolated gate driver that can drive IGBTs and MOSFETs. It has 4.0A peakoutput current capability with maxim output driver supply voltage of 30V. It has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor programmable dead time control, an DIS pin, and under voltage lock out (UVLO) for both input and output voltages.

Under Voltage Lockout

The has under voltage lock out (UVLO) protection feature on each driver power supply voltage between the VDDA (VDDB) and GNDA (GNDB) pins. When the VDDx voltage is lower than VUVLO_VDDX_R, during device start up or lower than VUVLO_VDDX_F, after start up, the VDDA (VDDB) UVLO feature holds the driver output low,regardless of the status of the input pins. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply. The also monitors the input power supply and there is an internal under voltage lock out protection feature on the VDDI. The driver outputs (OUTA and OUTB) are hold low when the voltage on the VDDI is lower than VUVLO_VDDI_R during start up or lower than VUVLO_VDDI_F after start up. There is a hysteresis on the VDDI UVLO feature to prevent glitch due the noise on the VDDI power supply.

Disable Input Function

When the DIS is pulled high, the OUTA and OUTB are pulled low regardless of the states of INA and INB. Whenthe DIS pin is pulled low, the VOA and VOB are allowed for normal operation and controlled by the INA and INB.The DIS input has no effect if VDDI is below its UVLO threshold and OUTA,OUTB remain low. There is an internalpull down resistor on the DIS pin.

Control Input and Output Logic

The INA and INB input controls the corresponding output channel,OUTA and OUTB.A logic high signal on INA (INB)causes the output of OUTA(OUTB) to go high. And a logic low on INA (INB) causes the output of OUTA(OUTB) togo low.

INA	INB	DIS	VDDI UVLO	VDDA UVLO	VDDB UVLO	OUTA	OUTB	Notes
H	L	L	NO	NO	X	H	L	
L	H	L	NO	X	NO	L	H	
L	L	L	NO	X	X	L	L	
H	H	L	NO	NO	NO	H	H	Dual driver
H	H	L	NO	NO	NO	L	L	Half bridge
X	X	H	NO	NO	NO	L	L	Device disabled
X	X	X	YES	NO	NO	L	L	VDDI UVLO activated
X	H	L	NO	YES	X	L	X	VDDA UVLO activated
H	X	L	NO	NO	YES	X	L	VDDB UVLO activated

Truth table

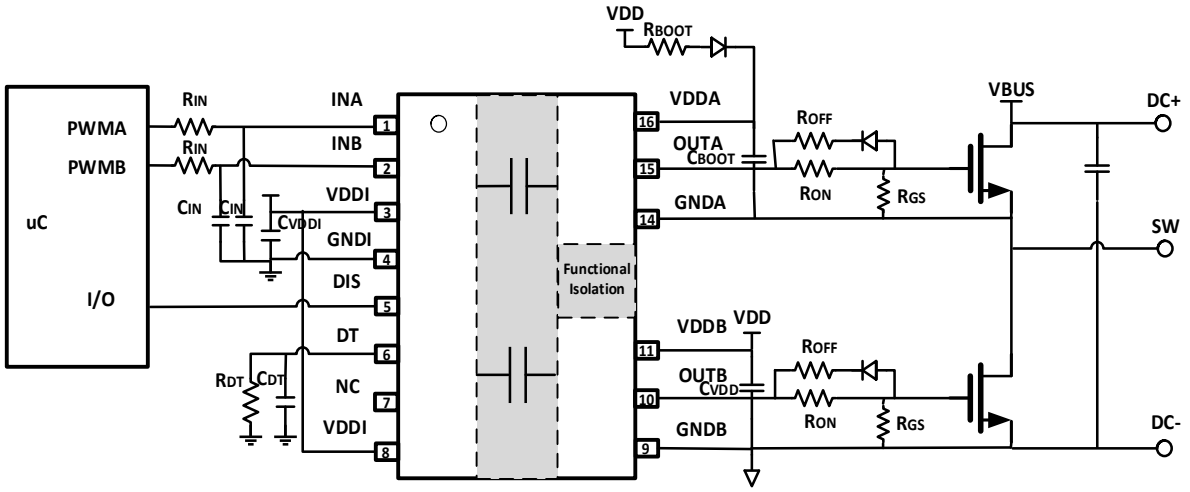
Dead-time Program

For the high side/low side configuration driver, there is a dead-time between OUTA and OUTB.The dead-time delay (tDT) is programmed by a resistor (RDT) connected from the DT input to ground and it can be calculated with below equation.

$$tDT\ [\text{ns}] \approx 10\times RDT\ [\text{k}\quad]$$

Here, tDT is the dead-time delay, RDT is the resistance value between DT and ground.
The DT pin can be connected to VDDI or left floating to provide a nominal dead time at approximately 10 ns.
A bypassing capacitor is recommended to be put between DT and GNDI to achieve better noise immunity.

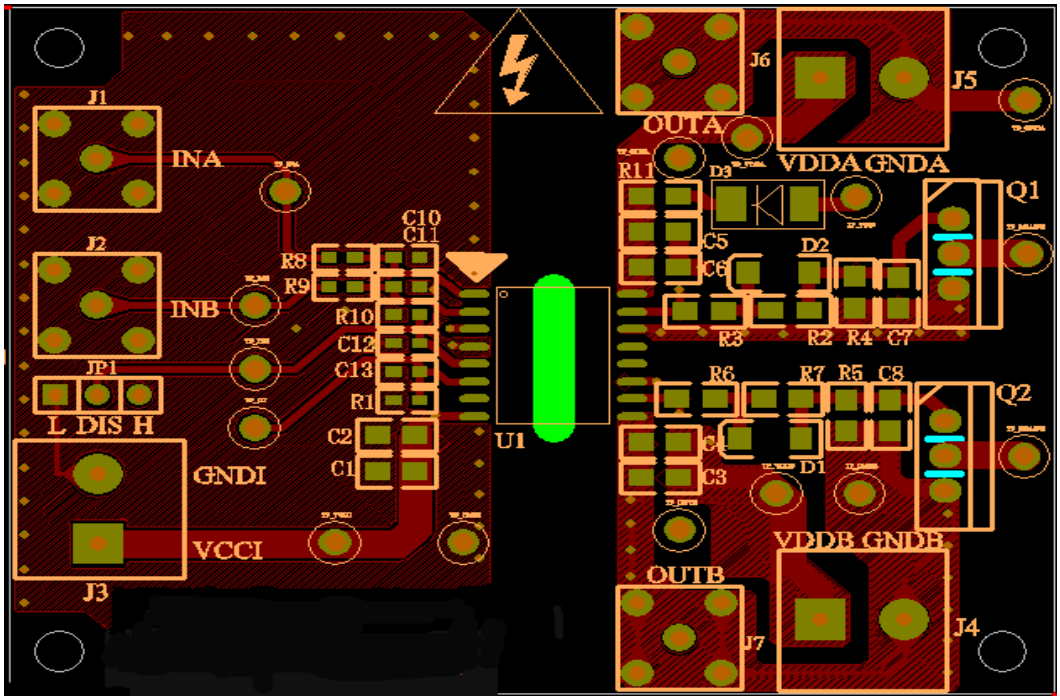
Application Information



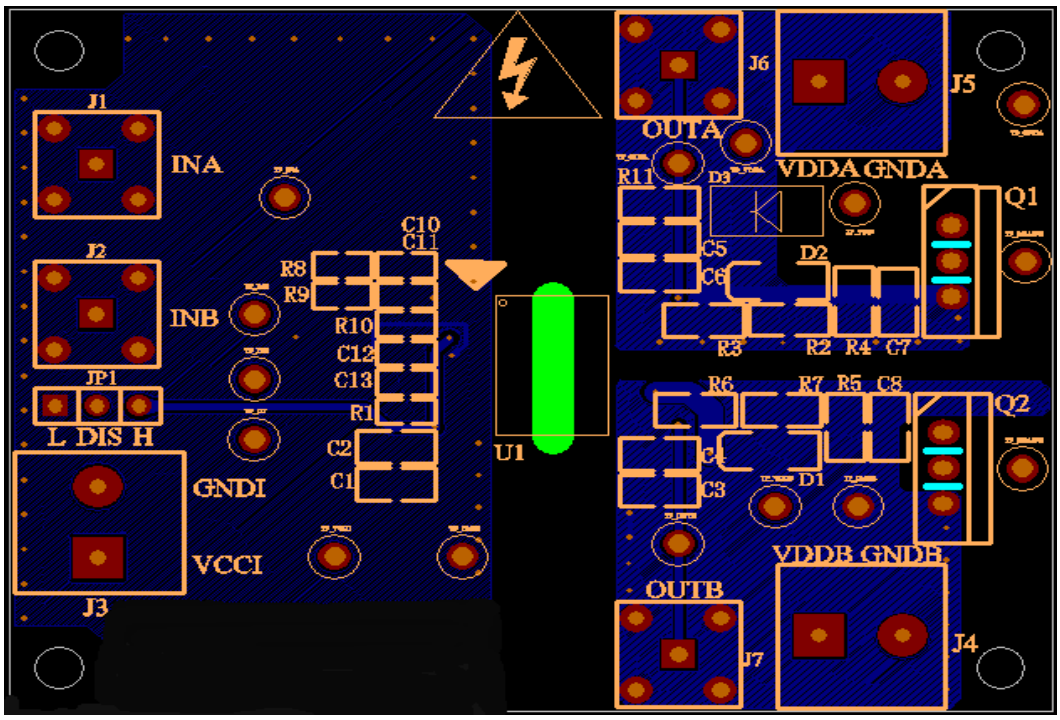
Typical Application Schematic

Parameter	Value	Units
VDDI	5	V
VDDA/VDDB	12	V
Input signal amplitude	5	V
Switching frequency(fs)	10~100	KHz
Dead time	200	nS
RDT	20	kΩ
CDT	2.2	nF
RIN	51	Ω
CIN	33	pF
RON	10	Ω
ROFF	-	Ω
RBOOT	22	Ω
RGS	10	kΩ
CVDDI	10	uF
CVDD	10	uF
CBOOT	10	uF

Recommended Design



PCB Top View



PCB Bottom View

Insulation Characteristics

	Value	Note
Installation class:		
mains≤ 150Vrms	I-IV	
mains≤ 300Vrms	I-IV	
mains≤ 600Vrms	I-IV	
mains≤ 1000Vrms	I-III	
climatic class	40/125/21	
pollution degree	2	
Clearance (mm)	8	
Creepage (mm)	8	
D_{TI}(um)	>20	
C_{TI}	600	
DIN EN IEC 60747-17 (VDE 0884-17):2021-10		
V_{IORM} (Vpeak)	1420	
V_{PR} (Vpeak)	2272	Method A, VPR = 1.6xV_{IORM}, 1s ,qpd< 5pC
V_{PR} (Vpeak)	2663	Method B, VPR = 1.875xV_{IORM}, 1s ,qpd< 5pC
V_{IOTM} (Vpeak)	5000	
V_{IOSM} (Vpeak)	5000	
R_{IO} (ohms)	>10e9	
UL1577		
V_{ISO} 1min (Vrms)	5700	
V_{ISO} 1s (Vrms)	6840	

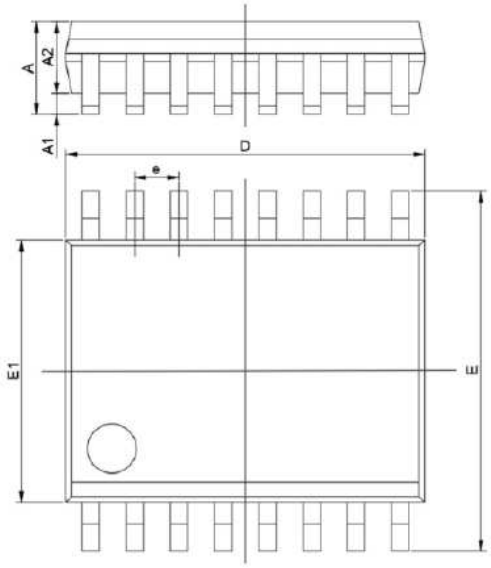
SOW-16 Insulation Characteristics

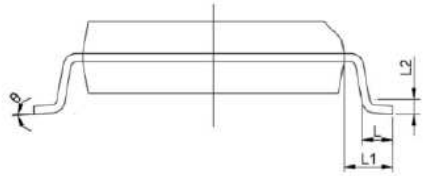
Certification Information

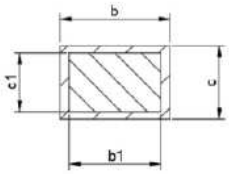
Certification Level		Industrial [1] (per JEDEC JESD 47E)
		The Series ICs have passed JEDEC's certification
Moisture Sensitivity Level		MSL1 [2] (per IPC/JEDEC J-STD-020C)
ESD	MM Model	Class B (Per JEDEC standard EIA/JESD22-A115)
	HBM Model	Class 2 (Per EIA/JEDEC standard JESD22-A114)
IC Latch-up Test		Class Level 1 A (Per JESD78A)
RoHS Compliant		YES

Package Outline Dimensions

SOW-16







Dimension	MIN	MAX
A	-	2.65
A1	0.1	0.3
A2	2.05	-
b	0.31	0.51
b1	0.27	0.48
c	0.1	0.33
c1	0.1	0.3
E	10.3BASIC	
E1	7.5BASIC	
e	1.27BASIC	
L	0.4	1.27
L1	1.4REF	
L2	0.25BASIC	
θ	0	8
D	10.3	

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