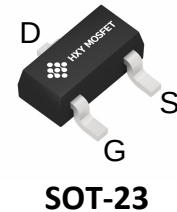




Description

The SI2351DS-T1-GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.



General Features

$V_{DS} = -20V, I_D = -2.3A$

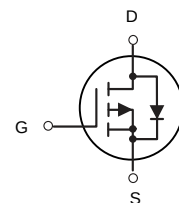
$R_{DS(ON)} < 115m\Omega @ V_{GS} = -4.5V$

$R_{DS(ON)} < 152m\Omega @ V_{GS} = -2.5V$

Application

PWM applications

Load switch



P-Channel MOSFET

Ordering Information

Product ID	Pack	Marking	Qty(PCS)
SI2351DS-T1-GE3	SOT-23	A1SHB	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous	-2.3	A
I_{DM}	Drain Current-Pulsed (Note 1)	-10	A
P_D	Maximum Power Dissipation	0.7	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	178	°C/W



Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-20		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.7	-1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-2A		95	115	mΩ
		V _{GS} =-2.5V, I _D =-1.8A		125	152	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-2A	4	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, F=1.0MHz	-	285	-	PF
Output Capacitance	C _{oss}		-	58	-	PF
Reverse Transfer Capacitance	C _{rss}		-	32	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-10V, R _L =5Ω V _{GS} =-4.5V, R _{GEN} =3Ω	-	9.8	-	nS
Turn-on Rise Time	t _r		-	4.9	-	nS
Turn-Off Delay Time	t _{d(off)}		-	20.5	-	nS
Turn-Off Fall Time	t _f		-	7	-	nS
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-2A, V _{GS} =-4.5V	-	2.9	-	nC
Gate-Source Charge	Q _{gs}		-	0.45	-	nC
Gate-Drain Charge	Q _{gd}		-	0.75	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-2A	-	-	-1.2	V
Diode Forward Current (Note 2)	I _S		-	-	-2.0	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



Typical Electrical and Thermal Characteristics

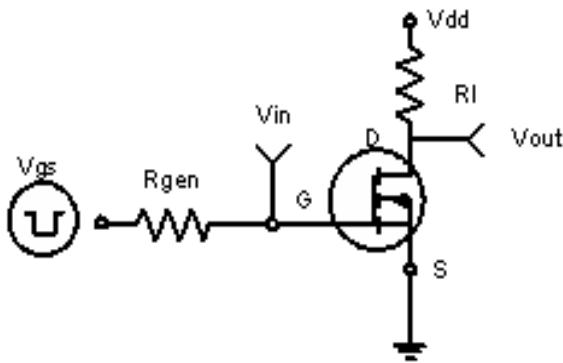


Figure 1: Switching Test Circuit

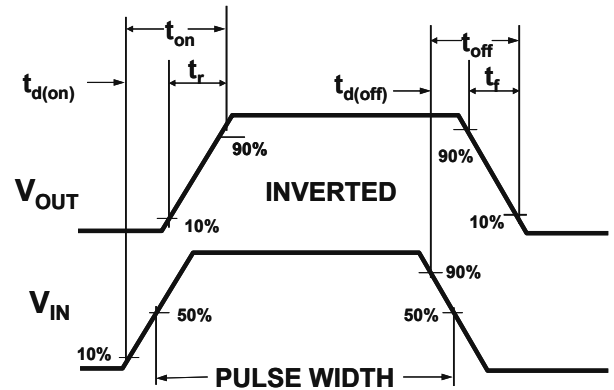


Figure 2: Switching Waveforms

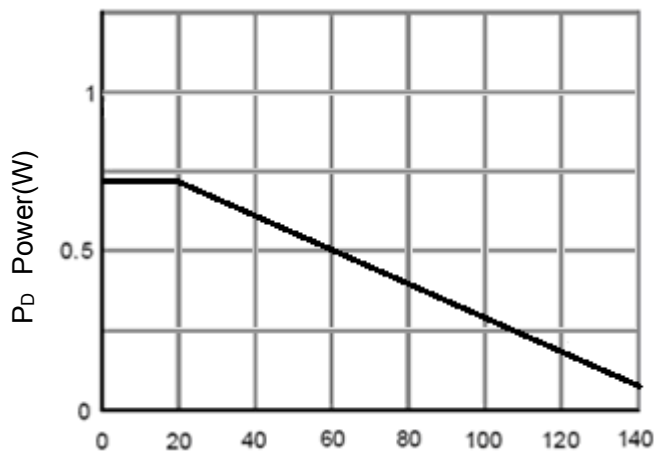


Figure 3 Power Dissipation

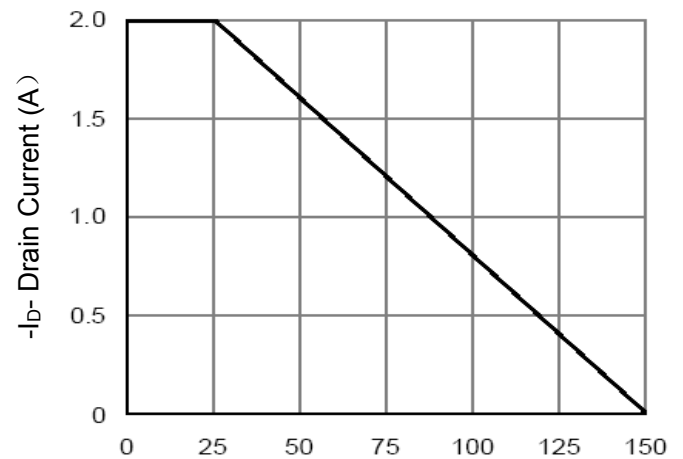


Figure 4 Drain Current

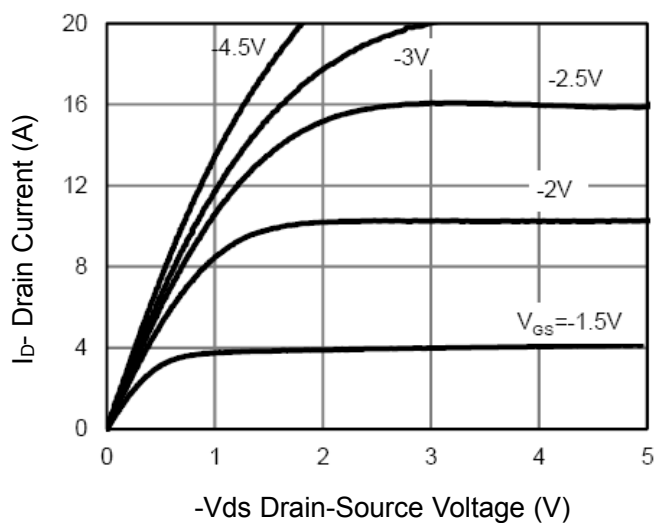


Figure 5 Output Characteristics

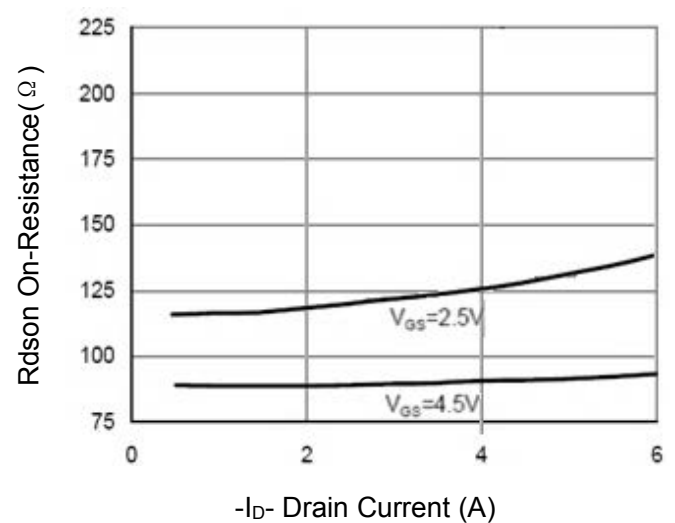


Figure 6 Drain-Source On-Resistance

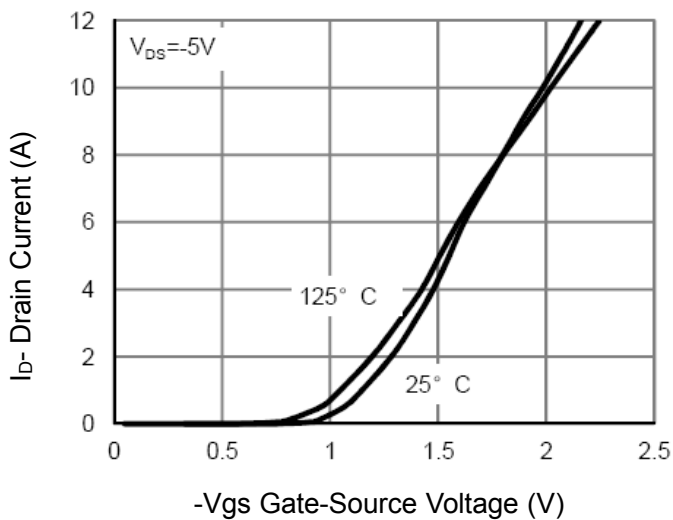


Figure 7 Transfer Characteristics

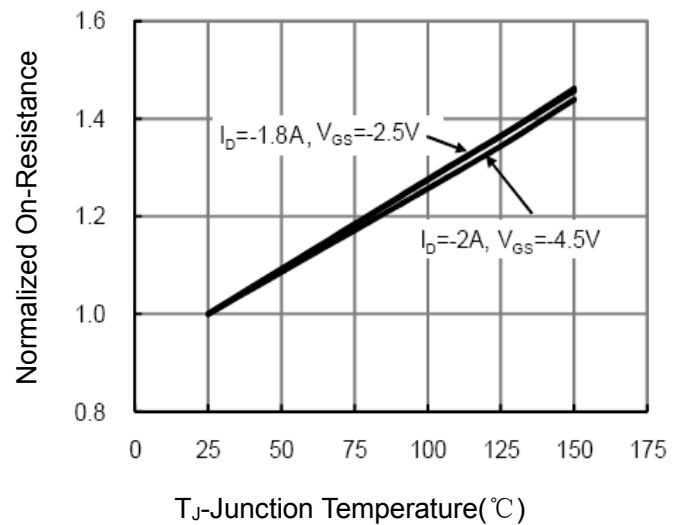


Figure 8 Drain-Source On-Resistance

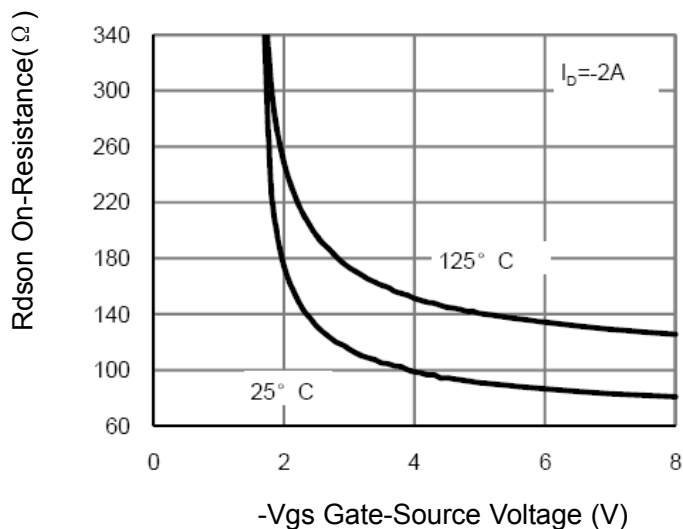


Figure 9 Rdson vs Vgs

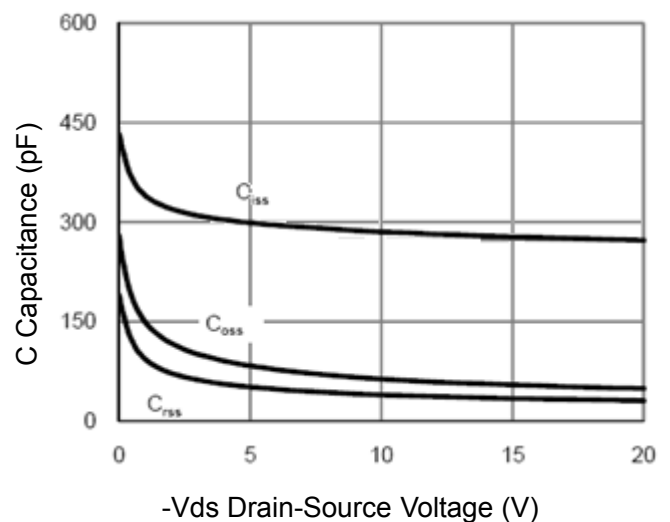


Figure 10 Capacitance vs Vds

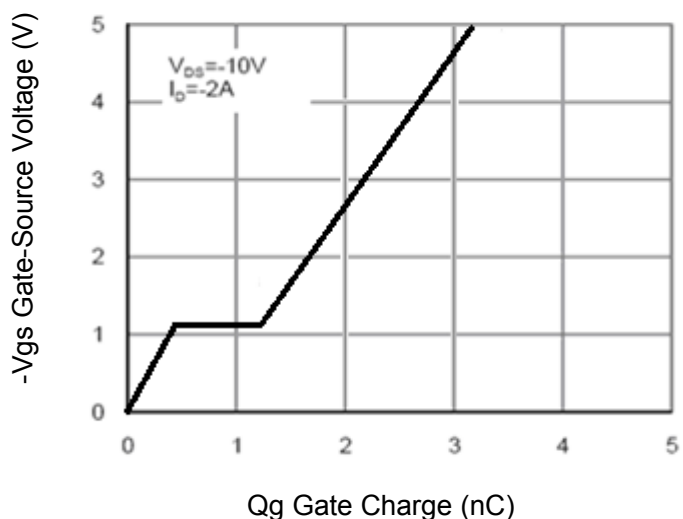


Figure 11 Gate Charge

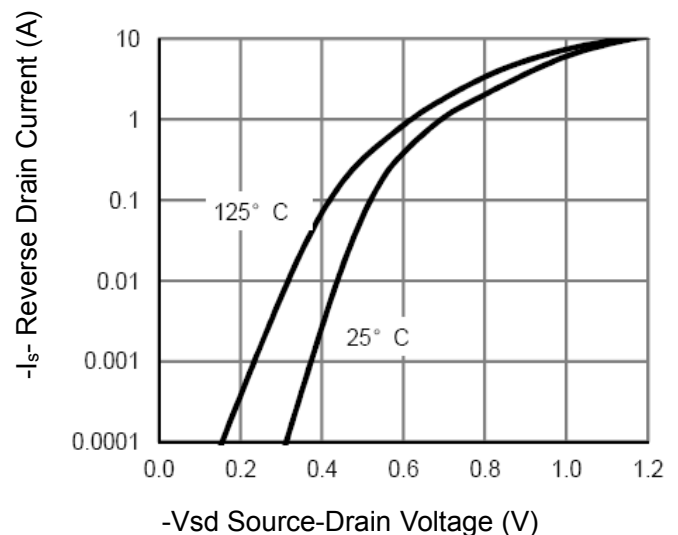


Figure 12 Source- Drain Diode Forward

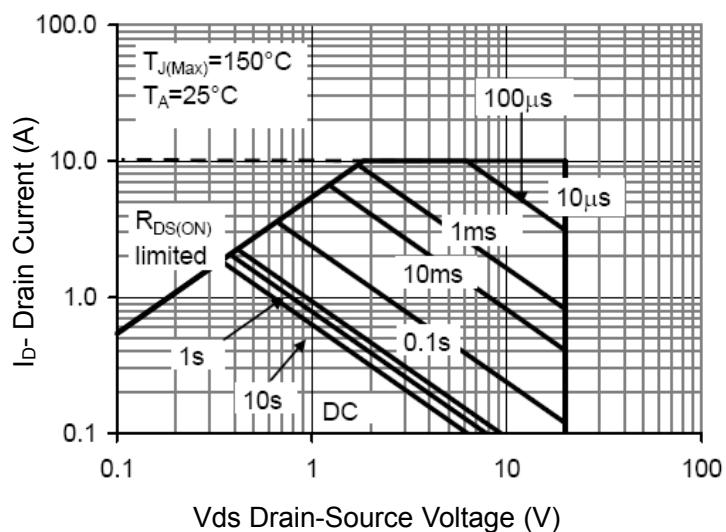


Figure 13 Safe Operation Area

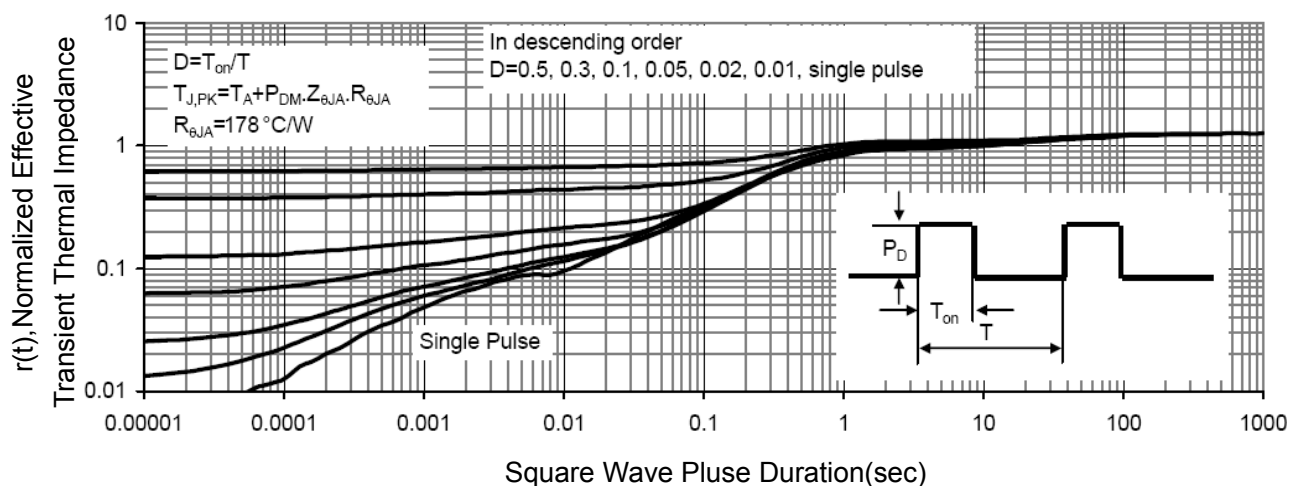
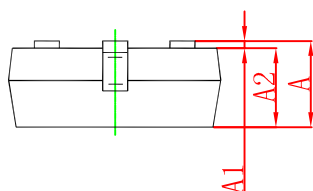
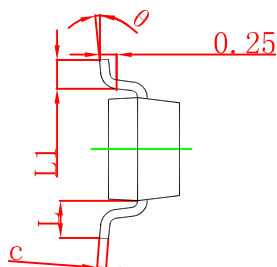
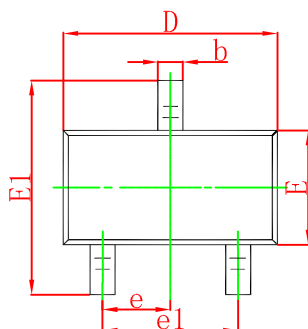


Figure 14 Normalized Maximum Transient Thermal Impedance

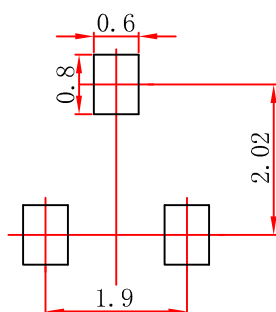


SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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