



Description

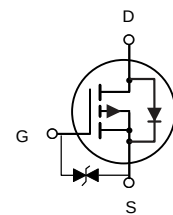
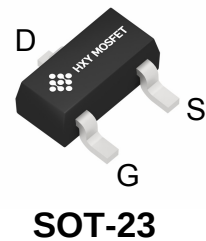
The DMP510DL-7 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

$V_{DS} = -50V, I_D = -0.1A$
 $R_{DS(ON)} < 5\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 6\Omega @ V_{GS} = -4.5V$
ESD Rating: 2000V HBM

Application

Power switching application
Hard switched and high frequency circuits
DC-DC converter



P-Channel MOSFET

Ordering Information

Product ID	Pack	Marking	Qty(PCS)
DMP510DL-7	SOT-23	PD	3000

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-50	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-0.1	A
Pulsed Drain Current	I_{DM}	-0.5	A
Maximum Power Dissipation	P_D	0.35	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$
Thermal Resistance ,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	$^\circ C/W$



Electrical Characteristics (Ta=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} =0, I _D =250μA	-50			V
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.8		-2.0	V
I _{GSS}	Gate-body leakage current	V _{DS} =0, V _{GS} =±10V			±10	μA
I _{DSS}	Zero gate voltage drain current	V _{DS} =-50V, V _{GS} =0V			-10	μA
		V _{DS} =-40V, V _{GS} =0V			-100	nA
R _{DS(on)}	Drain-source on-resistance ^a	V _{GS} =-10V, I _D =-0.13A		2	5	Ω
		V _{GS} =-4.5V, I _D =-0.13A		2.5	6	Ω
g _{FS}	Forward transconductance ^a	V _{DS} =-25V, I _D =-0.13A	50			mS
V _{SD}	Diode forward voltage	I _S =-0.13A, V _{GS} =0V			-1.0	V
Dynamic						
C _{iss}	Input capacitance	V _{DS} =-25V, V _{GS} =0V, f=1MHz		25		pF
C _{oss}	Output capacitance			15		
C _{rss}	Reverse transfer capacitance ^b			3.5		
Switching ^b						
t _{d(on)}	Turn-on delay time	V _{GS} =-10V, V _{DS} =-15V I _D =-200mA, R _{GEN} =25Ω		16.7		nS
t _r	Rise time			8.6		
t _{d(off)}	Turn-off delay time			17.9		
t _f	Fall time			5.3		

Notes :

a. Pulse Test : Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to producing.



Typical Characteristics

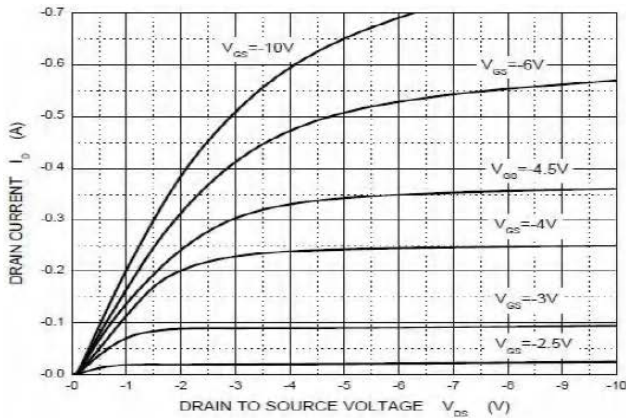


Figure1. Output Characteristics

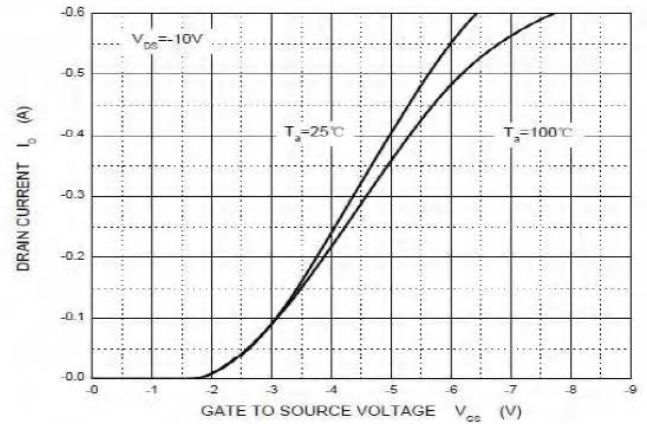


Figure2. Transfer Characteristics

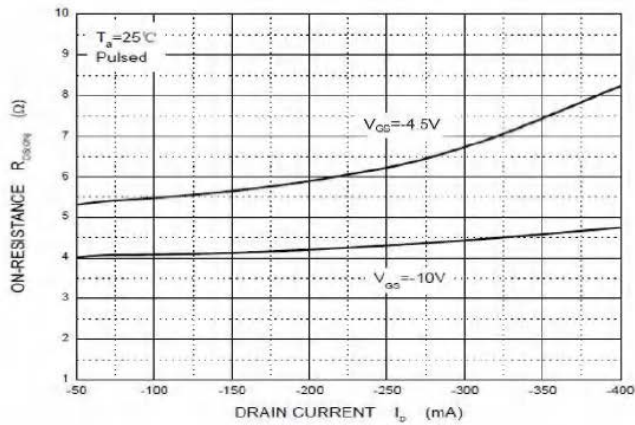


Figure3. Drain-Source on Resistance

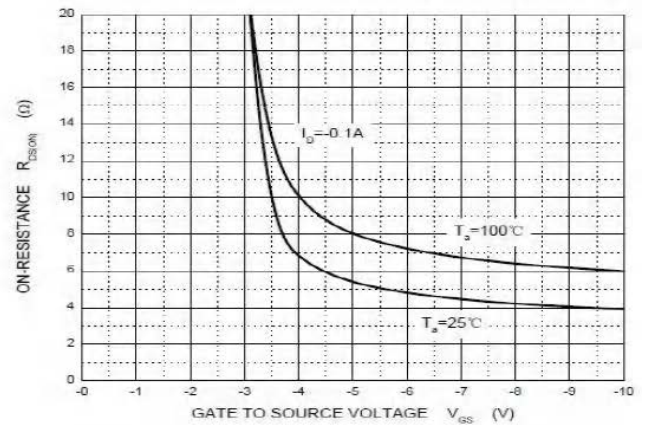


Figure4. Drain-Source on Resistance

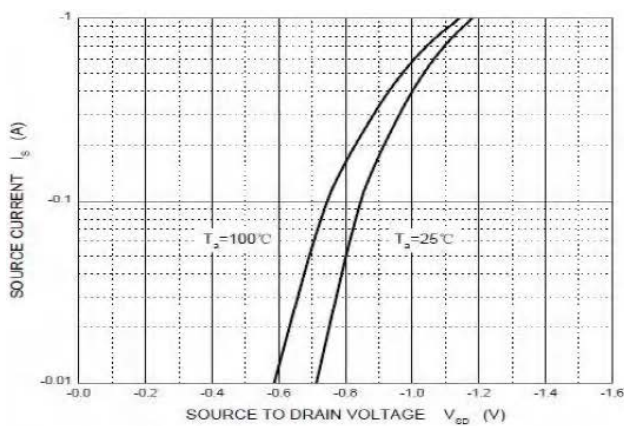


Figure5. Diode Forward Voltage vs. current

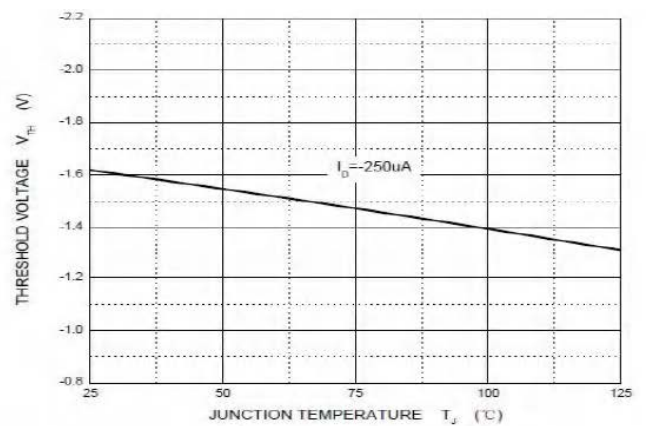
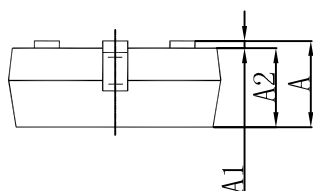
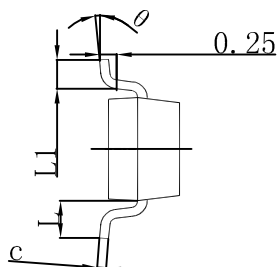
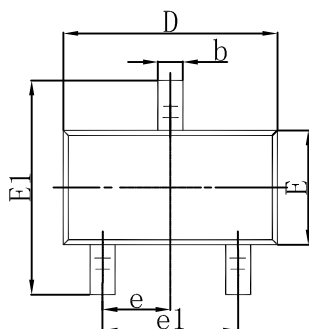


Figure6. Gate Threshold vs. Junction Temperature

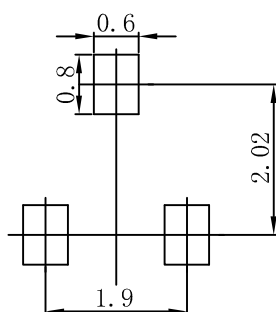


SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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