



Description

The DMP2070UQ-7 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

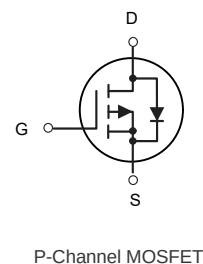
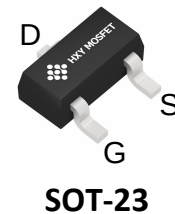
General Features

$V_{DS} = -20V, I_D = -5A$

$R_{DS(ON)} < 45m\Omega @ V_{GS}=4.5V$

Application

High power and current handing capability
Lead free product is acquired
Surface mount package
PWM applications
Load switch
Power management



Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMP2070UQ-7	SOT-23	HXY MOSFET	3000PCS

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous	-5	A
I_{DM}	Drain Current-Pulsed (Note 1)	-14	A
P_D	Maximum Power Dissipation	1.31	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	120	$^\circ C/W$



Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.014	---	$\text{V}/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V$, $I_D=-4.9A$	---	35	45	$\text{m}\Omega$
		$V_{GS}=-2.5V$, $I_D=-3.4A$	---	45	60	
		$V_{GS}=-1.8V$, $I_D=-2A$	---	65	85	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-0.4	---	-1.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.95	---	$\text{mV}/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-16V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	-1	μA
		$V_{DS}=-16V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V$, $I_D=-3A$	---	12.8	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V$, $V_{GS}=-4.5V$, $I_D=-3A$	---	10.2	14.3	nC
Q_{gs}	Gate-Source Charge		---	1.89	2.6	
Q_{gd}	Gate-Drain Charge		---	3.1	4.3	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10V$, $V_{GS}=-4.5V$, $R_G=3.3\Omega$, $I_D=-3A$	---	5.6	11.2	ns
T_r	Rise Time		---	40.8	73	
$T_{d(off)}$	Turn-Off Delay Time		---	33.6	67	
T_f	Fall Time		---	18	36	
C_{iss}	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	857	1200	pF
C_{oss}	Output Capacitance		---	114	160	
C_{rss}	Reverse Transfer Capacitance		---	108	151	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-4.9	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-14	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^{\circ}\text{C}$	---	---	-1	V
t_{rr}	Reverse Recovery Time	$I_F=-3A$, $di/dt=100A/\mu s$,	---	21.8	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25^{\circ}\text{C}$	---	6.9	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

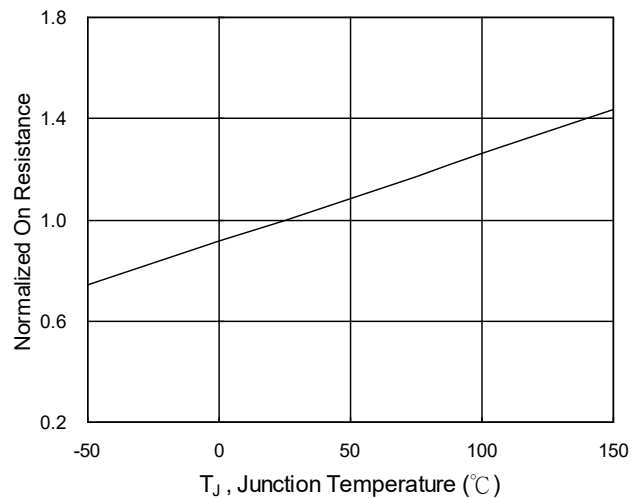
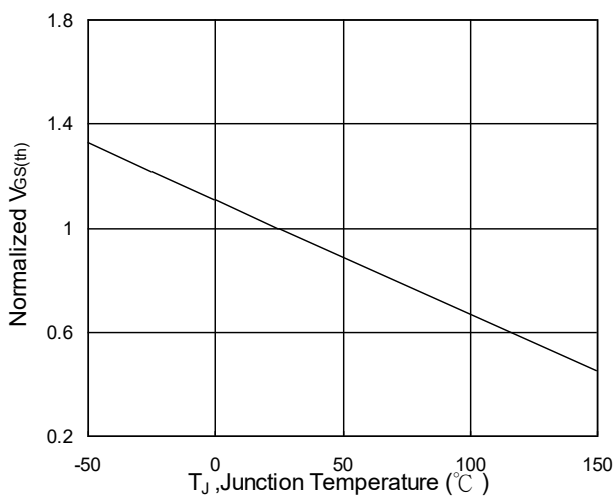
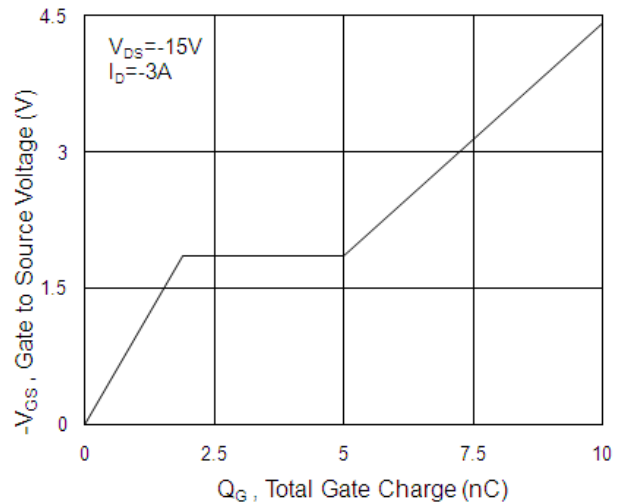
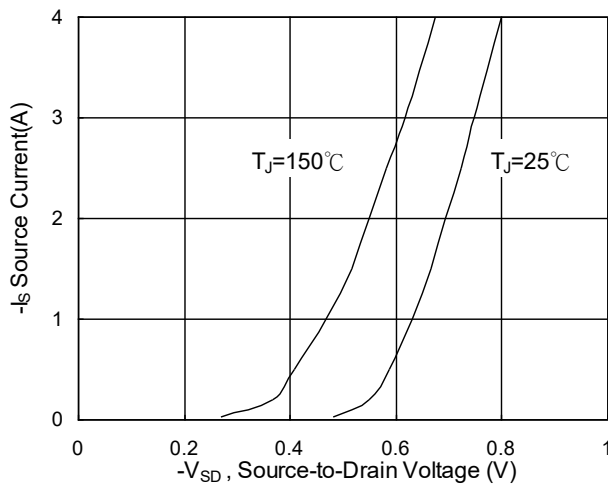
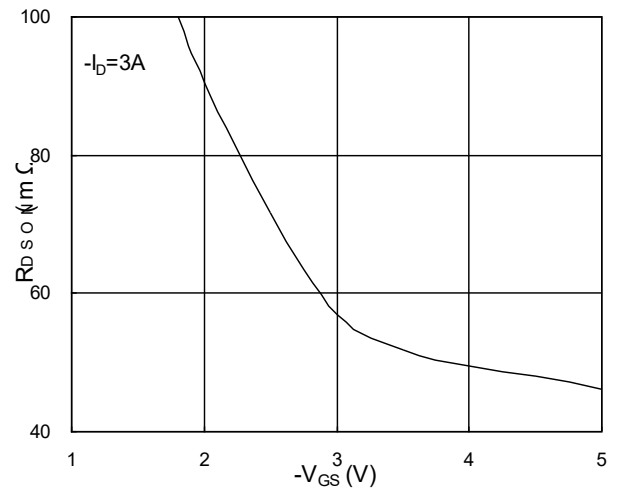
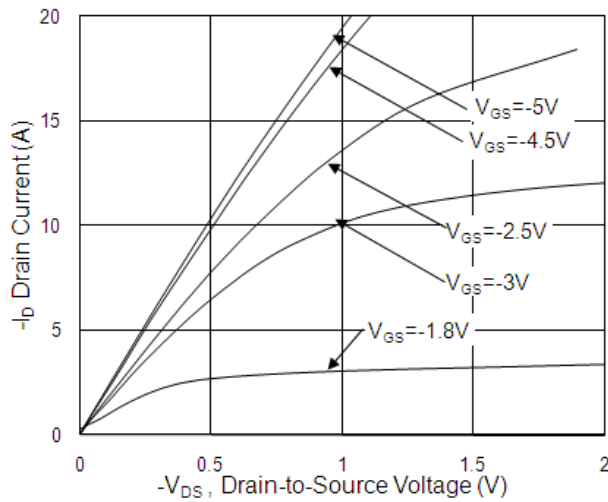
2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The power dissipation is limited by 150°C junction temperature

4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics



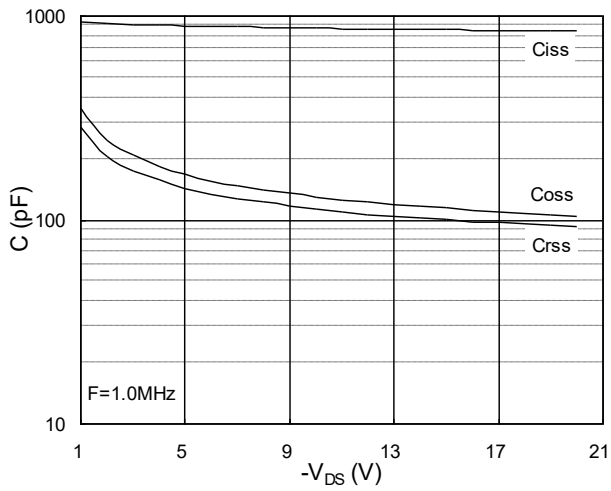


Fig.7 Capacitance

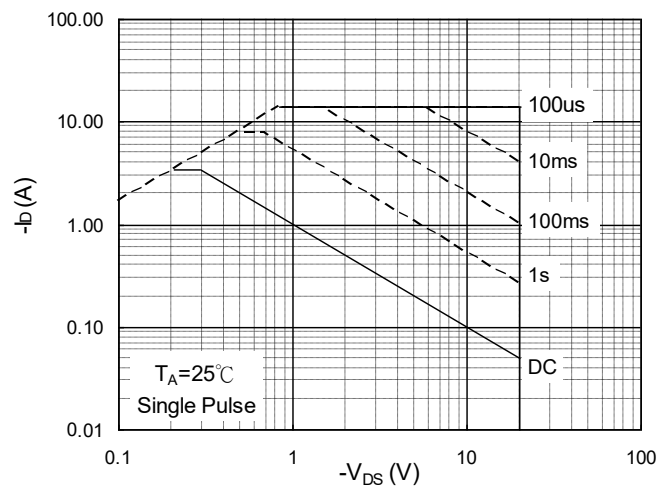


Fig.8 Safe Operating Area

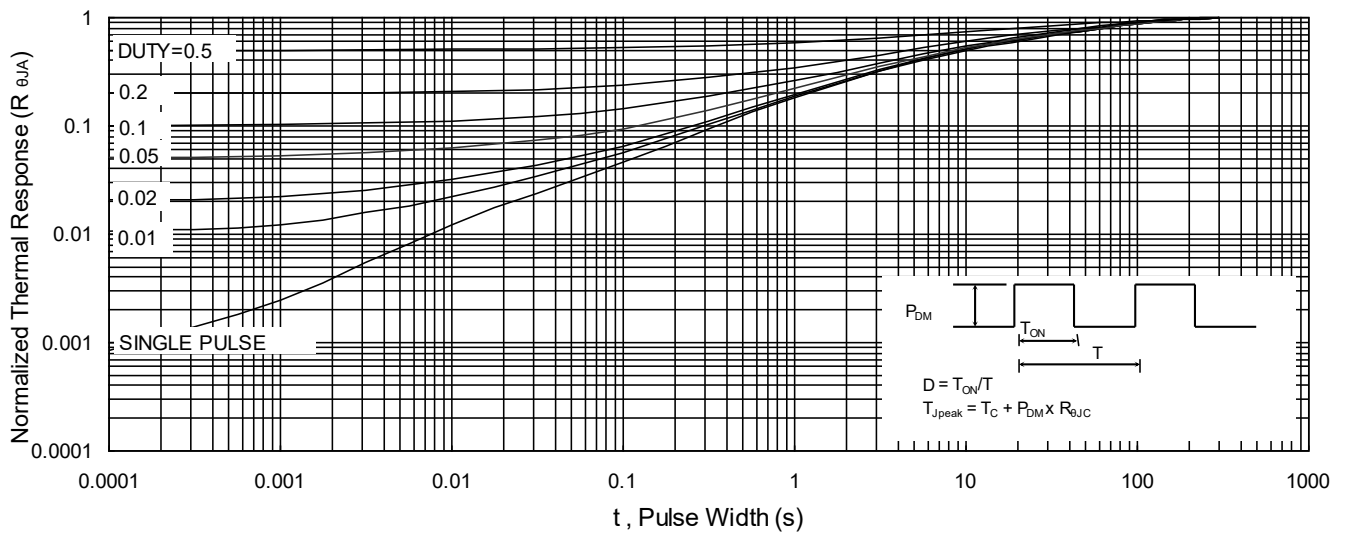


Fig.9 Normalized Maximum Transient Thermal Impedance

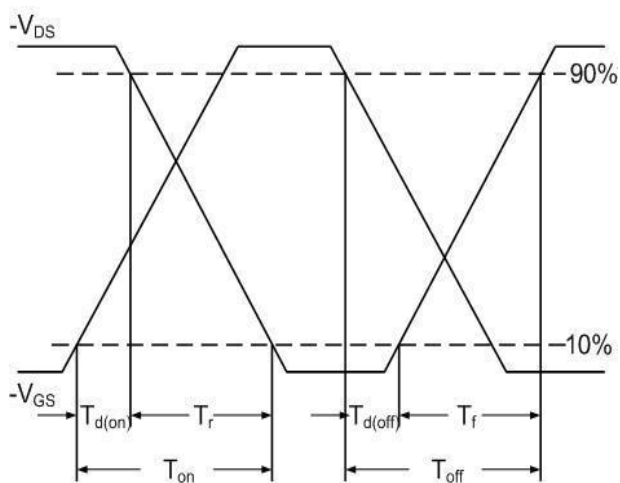


Fig.10 Switching Time Waveform

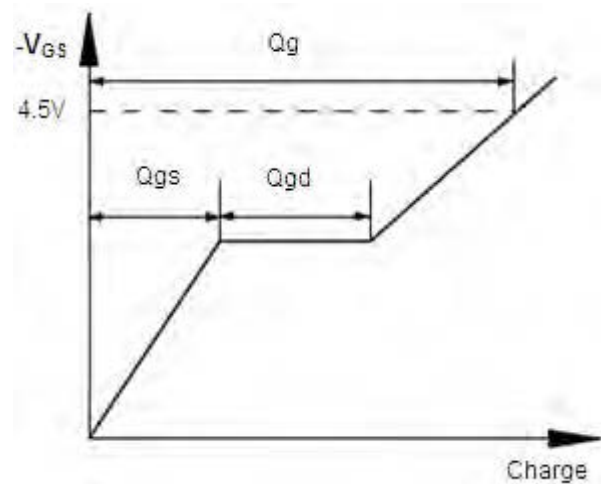
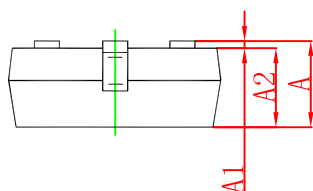
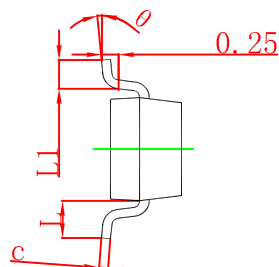
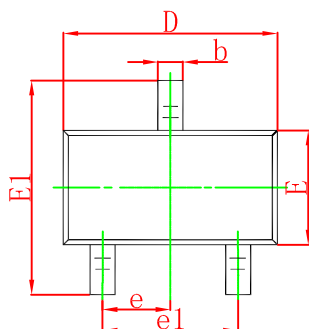


Fig.11 Gate Charge Waveform

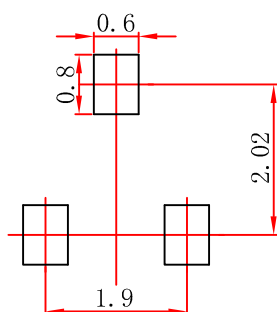


SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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