



Description

The SIR1309DP-T1-GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -30V$ $I_D = -70A$

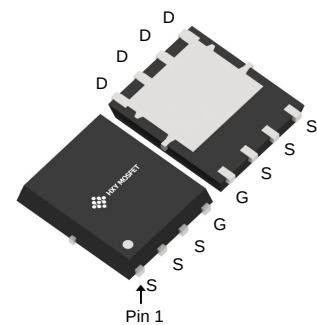
$R_{DS(ON)} < 8.8m\Omega$ $V_{GS} = -10V$

Application

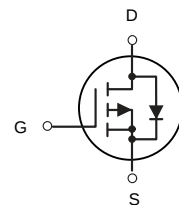
Battery protection

Load switch

Uninterruptible power supply



DFN5X6-8L



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SIR1309DP-T1-GE3	DFN5X6-8L	HXY MOSFET	5000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	-70	A
$I_D @ T_c=75^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	-40	A
I_{DM}	Pulsed Drain Current ²	-175	A
EAS	Single Pulse Avalanche Energy ³	31	mJ
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	31.2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	61	$^\circ C/W$



Electrical Characteristics($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30	-	-	V
Gate-body Leakage current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μA
	T _J =55°C			-	-	-5	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance ²		R _{DS(on)}	V _{GS} = -10V, I _D = -12A	-	6	8.8	mΩ
			V _{GS} = -4.5V, I _D = -8A	-	9	14	
Forward Transconductance		g _{fs}	V _{DS} = -5V, I _D = -20A	-	28	-	S
Dynamic Characteristics							
Input Capacitance		C _{iss}	V _{DS} = -15V, V _{GS} =0V, f =1MHz	-	4320	-	pF
Output Capacitance		C _{oss}		-	529	-	
Reverse Transfer Capacitance		C _{rss}		-	487	-	
Switching Characteristics							
Gate Resistance		R _g	V _{DS} = 0V, V _{GS} = 0V, f=1.0MHz	-	4.0	-	Ω
Total Gate Charge		Q _g	V _{GS} = -10V, V _{DS} = -15V, I _D = -15A	-	45	-	nC
Gate-Source Charge		Q _{gs}		-	8.5	-	
Gate-Drain Charge		Q _{gd}		-	12.8	-	
Turn-On Delay Time		t _{d(on)}	V _{GS} = -10V, V _{DD} = -15V, R _G = 2.5Ω, I _D = -15A	-	18.9	-	nS
Rise Time		t _r		-	15.7	-	
Turn-Off Delay Time		t _{d(off)}		-	64.8	-	
Fall Time		t _f		-	36.5	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ²		V _{SD}	I _S = -1A, V _{GS} = 0V	-	-	-1	V
Continuous Source Current ^{1,5}		I _S	V _G =V _D =0V , Force Current	-	-	-70	A

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1mH, I_{AS} = -25A$
- 4.The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Electrical And Thermal Characteristics (Curves)

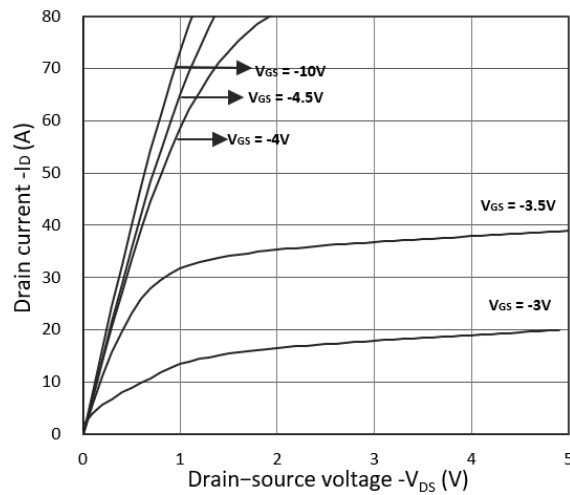


Figure 1. Output Characteristics

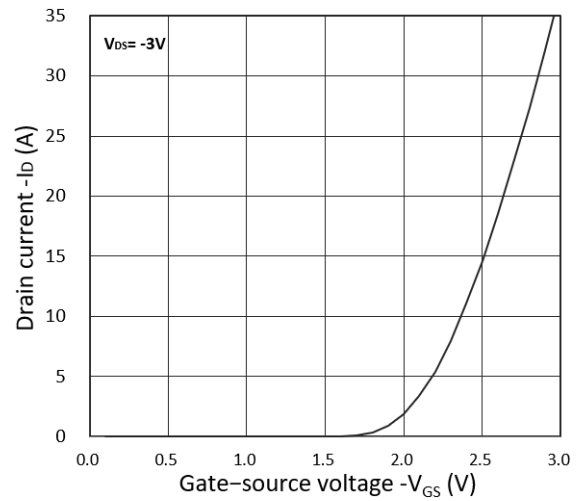


Figure 2. Transfer Characteristics

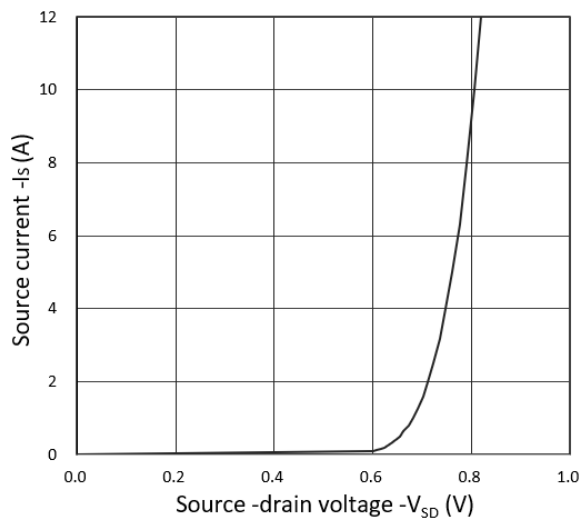


Figure 3. Forward Characteristics of Reverse

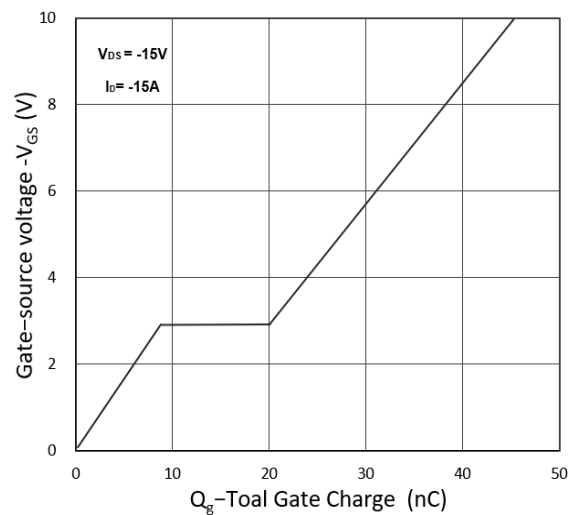


Figure 4. Gate Charge Characteristics

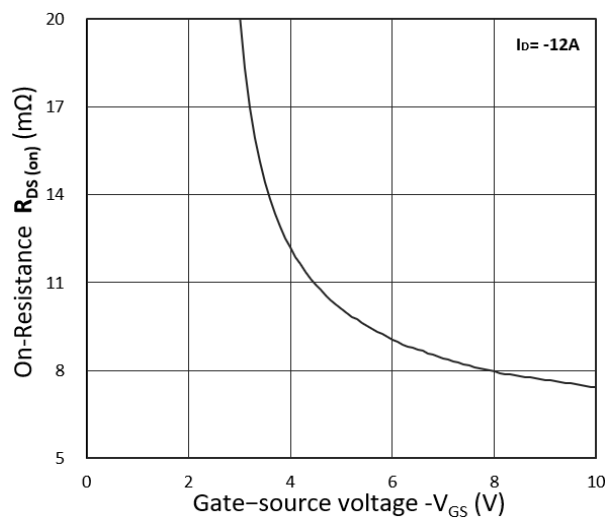


Figure 5. $R_{DS(on)}$ vs. V_{GS}

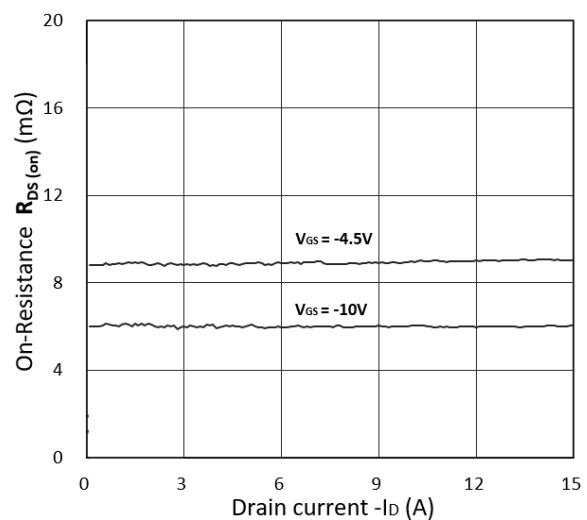


Figure 6. $R_{DS(on)}$ vs. I_D

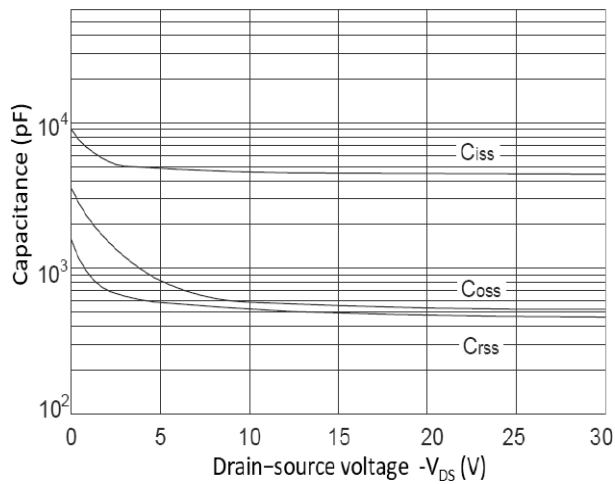


Figure 7. Capacitance Characteristics

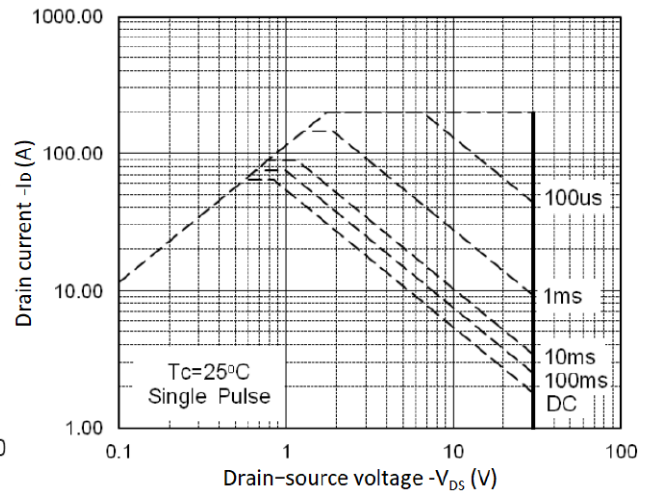


Figure 8. Safe Operating Area

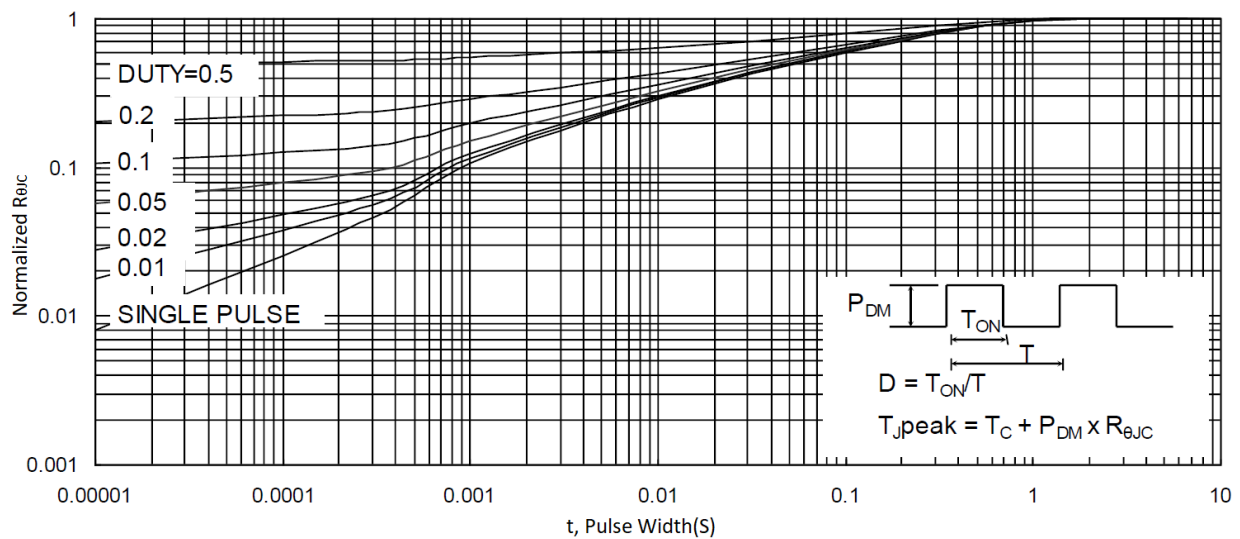


Figure 9. Normalized Maximum Transient Thermal Impedance

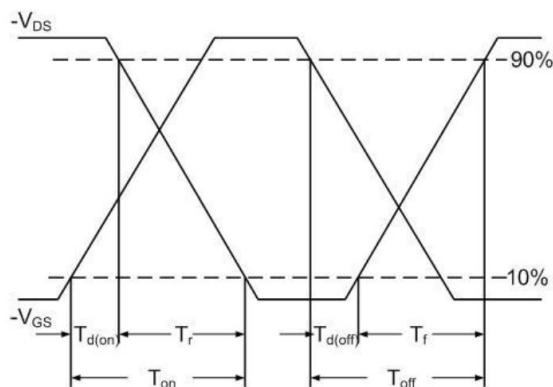


Figure 10. Switching Time Waveform

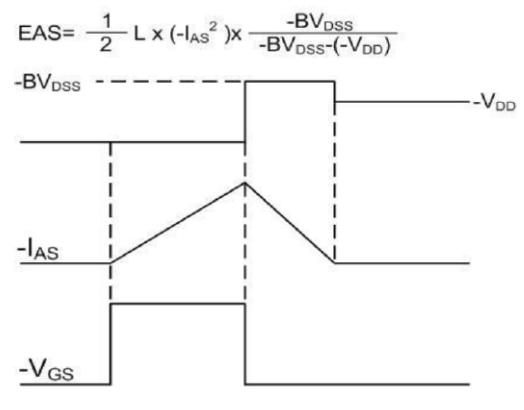
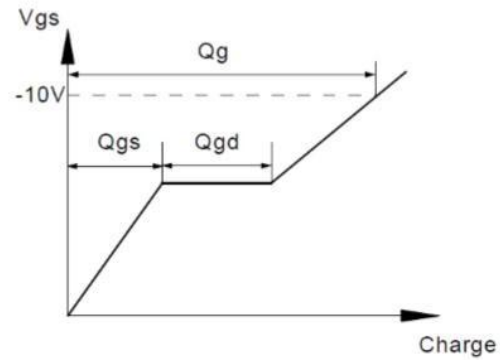
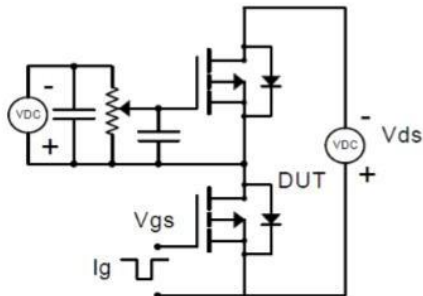


Figure 11. Unclamped Inductive Switching
Waveform

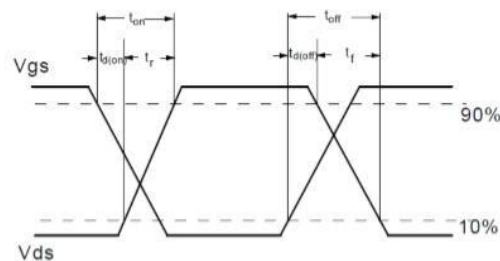
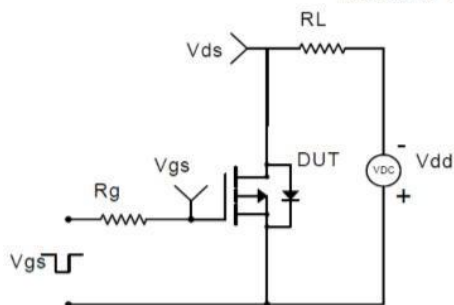


Test Circuit

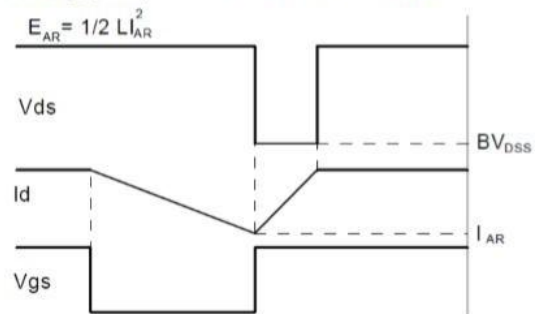
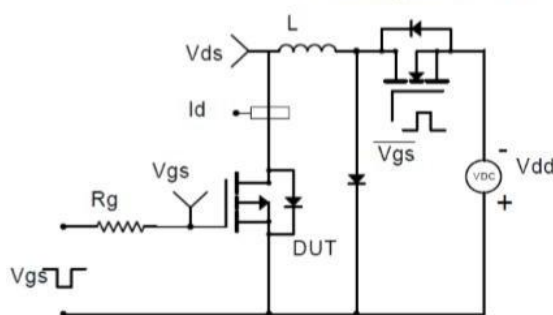
Gate Charge Test Circuit & Waveform



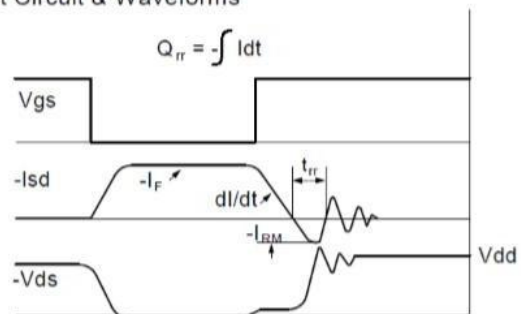
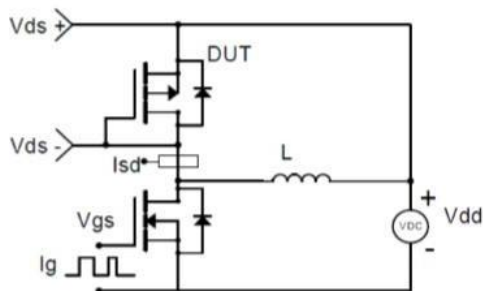
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

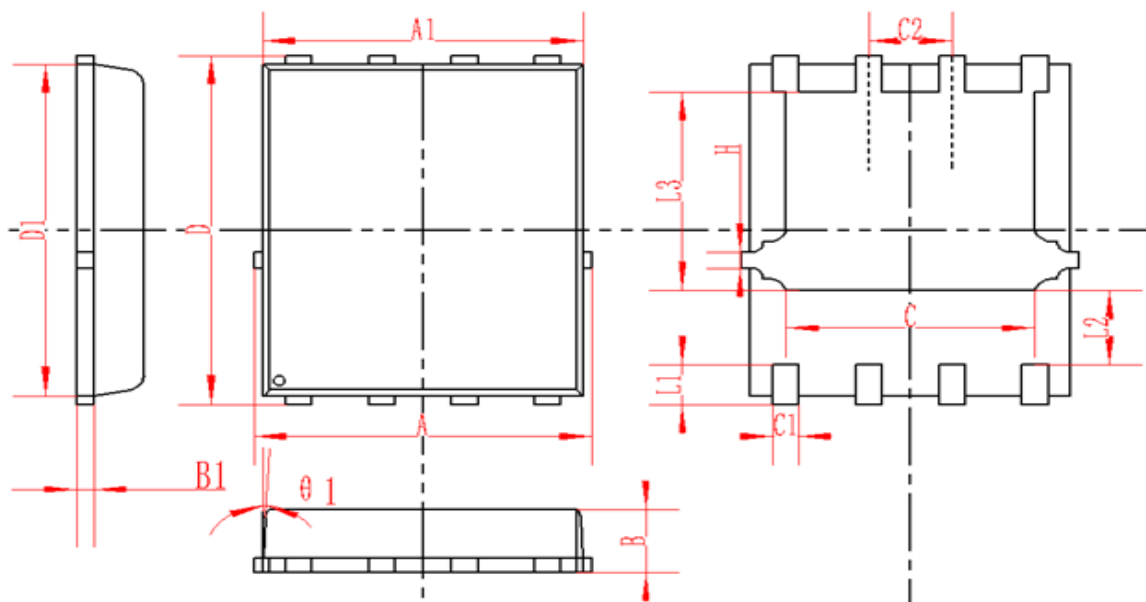


Diode Recovery Test Circuit & Waveforms





DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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