

概述

HT75xx-2 是一款采用 CMOS 技术的低压差线性稳压器。最大输出电流为 300mA 且允许的最高输入耐压为+48V。具有几个固定的输出电压，范围从+1.8V 到+5.0V。COMS 技术可确保其具有低压降和低静态电流的特性。

功能特点

- 低功耗
- 低压降
- 较低的温度系数
- 最高输入耐压电压: +48V
- 典型静态电流: 3uA
- 最大输出电流: 300mA
- 输出电压精度: $\pm 1\%$
- 封装类型: SOT-23-3L, SOT-89

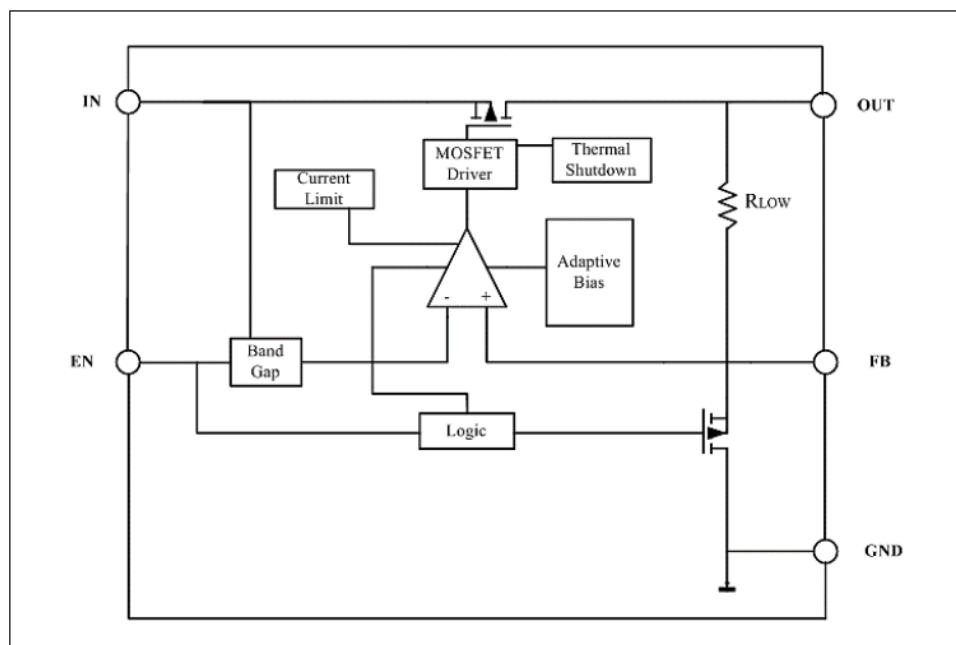
应用领域

- 电池供电设备
- 通信设备
- 音频/视频设备

选型表

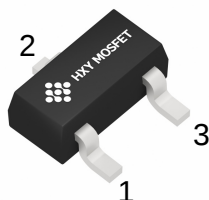
型号	输出电压	封装类型
HT7518-2	1.8V	SOT-23-3L SOT-89
HT7525-2	2.5V	
HT7530-2	3.0V	
HT7533-2	3.3V	
HT7536-2	3.6V	
HT7544-2	4.4V	
HT7550-2	5.0V	

电路功能框图

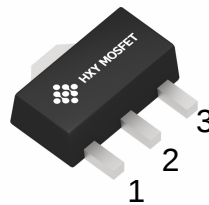




引脚图



SOT-23



SOT-89

引脚说明

引脚序号	引脚名称	说明
1	GND	地
2	VIN	电源输入脚
3	VOUT	输出脚，必须接 1uF 以上的电容到地

极限参数

	描述	数值	单位
Vin	输入电压	0~+45(Note1)	V
Vout	输出电压	1.8~5.0	V
T_{STG}	储存温度	-45~+140	°C
T_{WK}	工作温度	-40~+85	°C
ESD_{HBM}	人体模式	4000(Note2)	V
CDM	带电器件模式	1500(Note2)	V
Latch up	闩锁最大额度电流值	200(Note2)	mA

这里只强调额定功率，超过极限参数所规定的范围将对芯片造成损害，无法预期芯片在上述标示范围外的工作状态，而且若长期在标示范围外的条件下工作，可能影响芯片的可靠性。

Note1: 参考电气特性和应用信息。

Note2: 此系列产品的 ESD 保护通过以下测试方法：

根据 EIA/JESD22-A114 测试 ESD 人体模式。

根据 JESD22-C101 测试静电放电能力。

根据 JEDEC78 测试闩锁最大电流值。



建议工作条件

参数	描述	范围	单位
V_{IN}	输入电压	+2.5~+45	V
I_{OUT}	输出电流	0~300	mA
T_A	工作温度	-40~+85	°C
C_{IN}	输入端有极性电容	1~10	uF
C_{OUT}	输出端有极性电容	1~10	uF
ESR	输入输出端电容等效的电阻值	5~100	mΩ

热能信息

符号	参数	封装类型	最大值	单位
θ_{JA}	热阻（与环境连接）（假设无环境气流、无散热片）	SOT-23-3L	360	°C/W
		SOT-89	135	°C/W
P_D	功耗	SOT-23-3L	0.2	W
		SOT-89	0.5	W

注： P_D 值是在 $T_A=25^\circ\text{C}$ 时测得。

电气特性

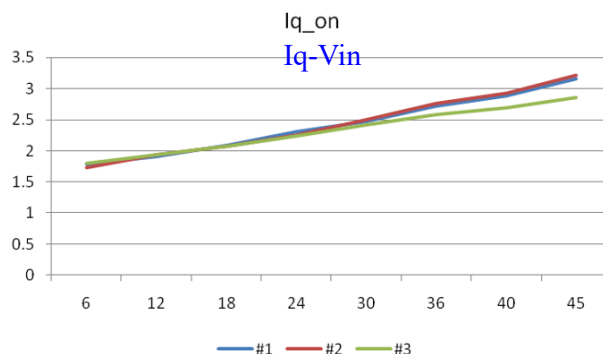
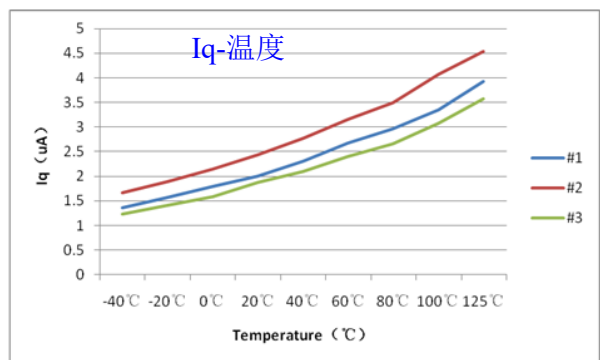
$T_A=25^\circ\text{C}$

符号	参数	测试条件	最小	典型	最大	单位
V_{IN}	输入电压	—	—	—	+45	V
V_{OUT}	输出电压	$T_A=+25^\circ\text{C}$	-1%		+1%	V
		$-40^\circ\text{C}\leq T_A\leq +85^\circ\text{C}$	-2%		+2%	V
V_{DROP}	压差 $I_{OUT}=300\text{mA}$	$V_{OUT}=1.8\text{V}$	—	1350	1650	mV
		$V_{OUT}=2.5\text{V}$	—	1150	1450	mV
		$V_{OUT}=2.8\text{V}$	—	1100	1400	mV
		$V_{OUT}=3.0\text{V}$	—	1050	1350	mV
		$V_{OUT}=3.3\text{V}$	—	1000	1300	mV
		$V_{OUT}=4.4\text{V}$	—	950	1250	mV
		$V_{OUT}=5\text{V}$	—	900	1200	mV
I_{OUT}	输出电流	$V_{IN}=V_{OUT}+2\text{V}$	—	300	—	mA
$Load_{Reg}$	负载调整率	$1\text{mA}\leq I_{OUT}\leq 300\text{mA}$ $V_{IN}=V_{OUT}+1\text{V}$	—	—	40	mV
I_{LMT}	极限电流	$V_{IN}=V_{OUT}+1\text{V}$	300	450	—	mA
I_{SHORT}	短路极限电流	$V_{OUT}=0\text{V}$	—	100	—	mA
I_Q	静态电流	无负载($I_{OUT}=0\text{mA}$)	—	3	4.0	uA
PSRR	电源抑制比	$V_{IN}=V_{OUT}+1\text{V}$, $I_{OUT}=20\text{mA}$ $f=1\text{KHz}$	—	60	—	dB
eN	Output Noise Voltage	$V_{IN}=V_{OUT}+1\text{V}$, $I_{OUT}=1\text{mA}$ $f=10\text{Hz}\sim 100\text{KHz}$ ($V_{OUT}=3\text{V}$) $C_{OUT}=1\text{uF}$	—	100	—	uVrms
R_{LOW}	输出放电电阻	$C_{IN}=4\text{V}$, $V_{EN}=0\text{V}$	—	70	—	Ω
$\frac{\Delta V_{OUT}}{\Delta V_{IN}\times V_{OUT}}$	输入电压调节率	$V_O+1\text{V}\leq V_{IN}\leq 45\text{V}$ $I_{OUT}=1\text{mA}$	—	—	0.2	%/V
$\frac{\Delta V_{OUT}}{\Delta T_A\times V_{OUT}}$	温度系数	$I_{OUT}=10\text{mA}$ $-40^\circ\text{C}\leq T_A\leq 85^\circ\text{C}$	—	100	—	ppm/°C

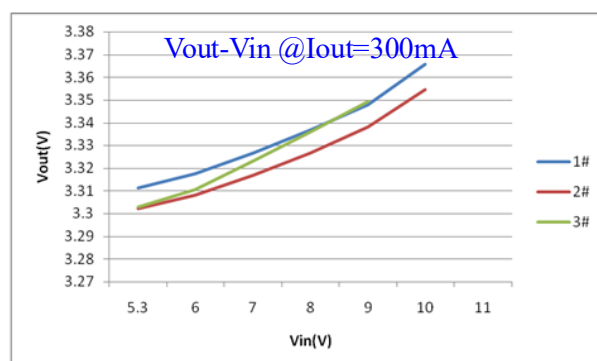
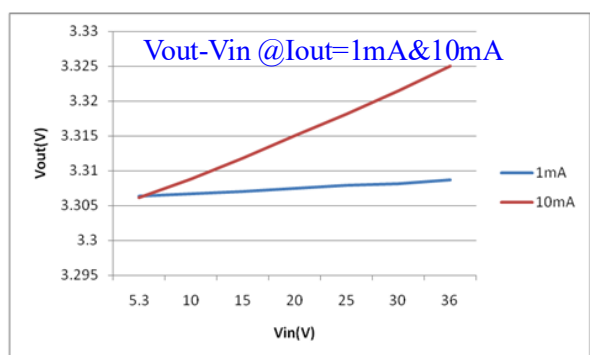
注：在 $V_{IN}=V_{OUT}+2\text{V}$ 与一个固定负载条件下使输出电压下降 2%，此时的输入电压减去输出电压就是 Dropout 电压。



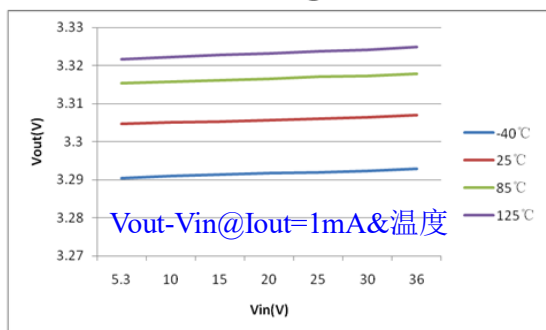
典型性能特征



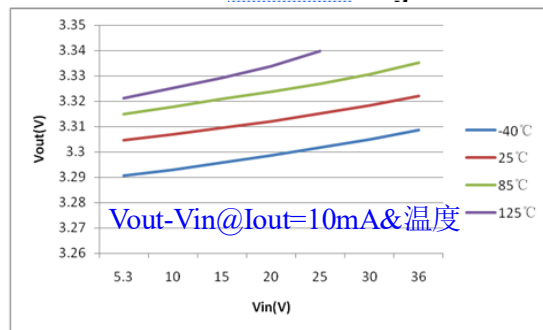
DC Supply Quiescent Current



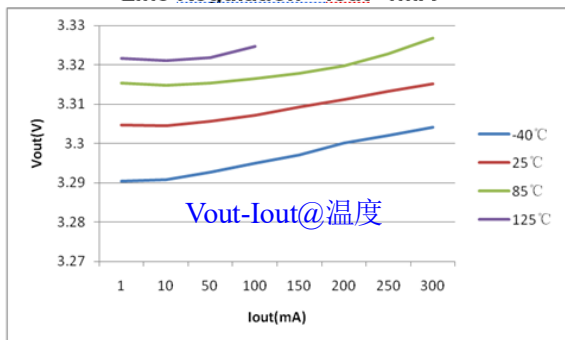
Line Regulation



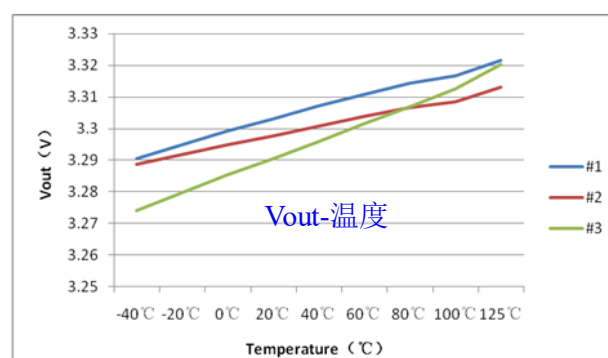
Iout=300mA Line Regulation



Line Regulation Iout=1mA

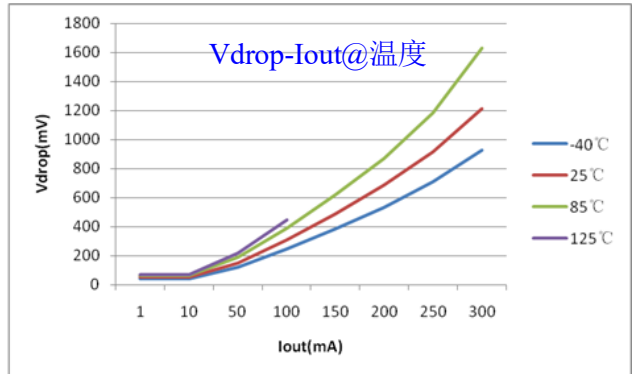
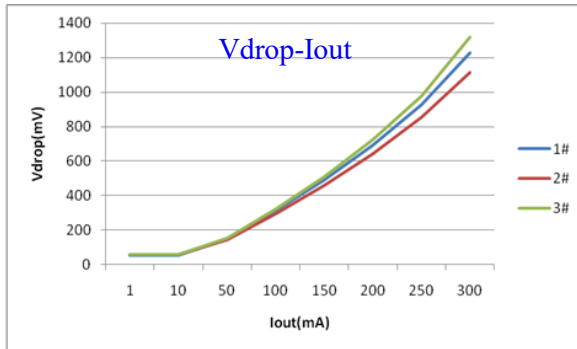


Line Regulation Iout=10mA

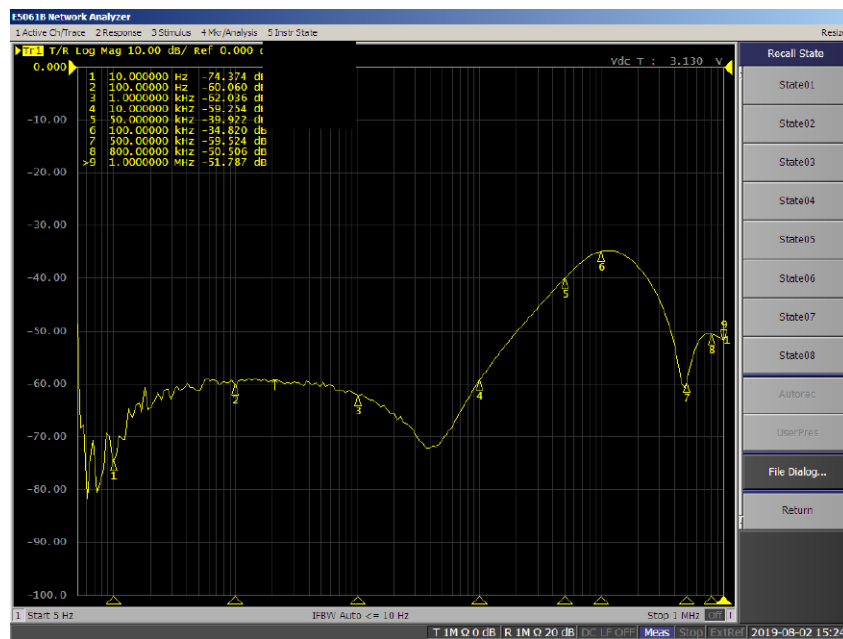


Load Regulation

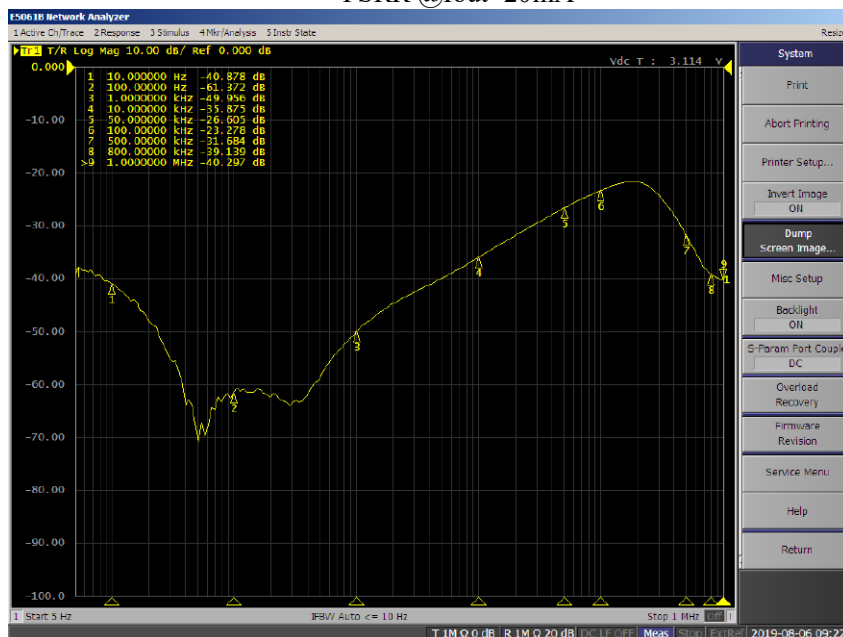
Output Voltage



PSSR:



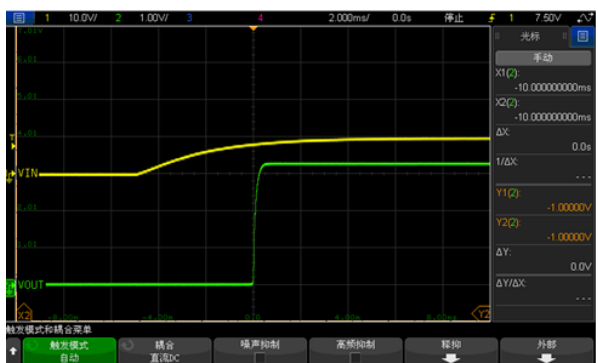
PSRR @Iout=20mA



PSRR @Iout=300mA



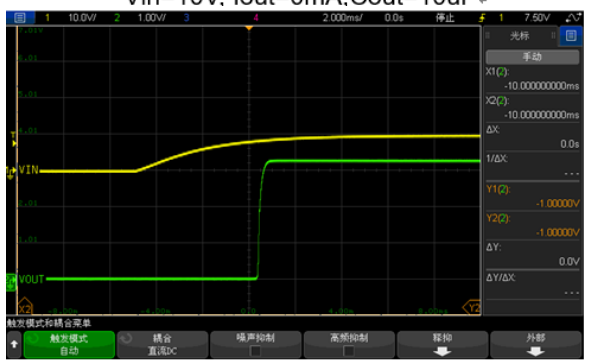
启动特性:



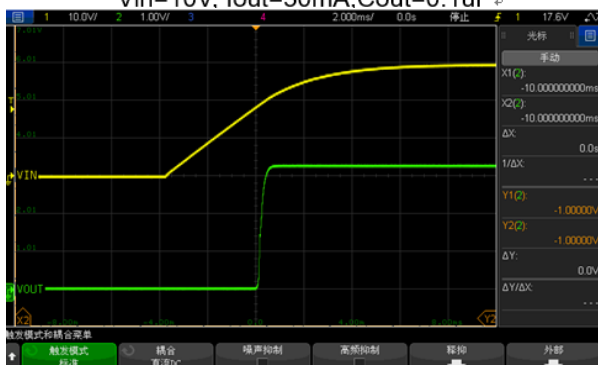
Vin=10V, Iout=0mA, Cout=0.1uF



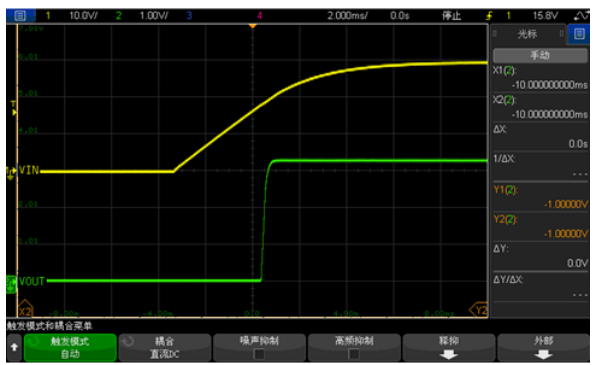
Vin=10V, Iout=0mA, Cout=10uF



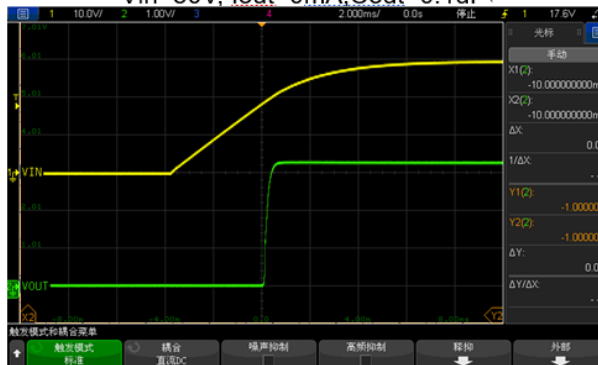
Vin=10V, Iout=30mA, Cout=0.1uF



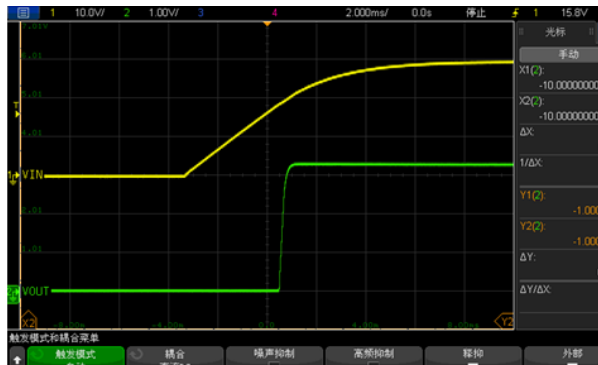
Vin=10V, Iout=30mA, Cout=10uF



Vin=30V, Iout=0mA, Cout=0.1uF



Vin=30V, Iout=0mA, Cout=10uF



Vin=30V, Iout=30mA, Cout=10uF

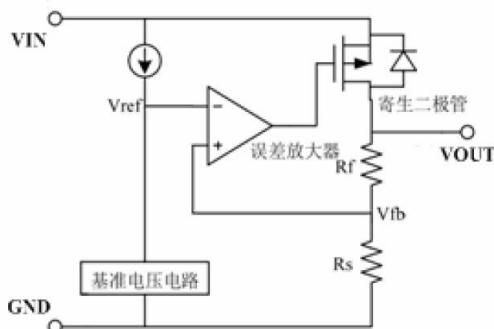


限流保护

具备限流功能，防止设备在过载或短路情况下损坏。该电流由内部感应晶体管检测。

功能描述

误差放大器根据反馈电阻 R_s 及 R_f 所构成的分压电阻的输入电压 V_{fb} 同基准电压 V_{ref} 相比较。通过此误差放大器向输出晶体管提供必要的门极电压，而使输出电压不受输入电压或温度变化的影响而保持一定。



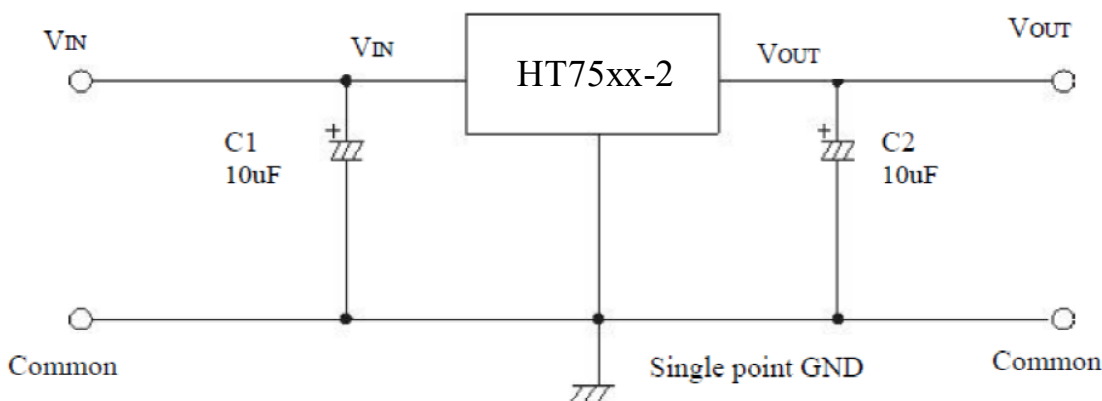
使用注意事项:

- 1) 电路内部使用了相位补偿电路和利用输出电容的 ESR 来补偿，所以输出到地建议接大于 1uF 的电容器。
- 2) 建议应用时输入和输出使用 10uF 有极性电容，并尽量将电容靠近 LDO 的 VIN 和 VOUT 脚位。
- 3) 注意输入和输出电压与负载电流的使用条件，避免 IC 内部的功耗(PD)超出封装允许的最大功耗值。

PD 的计算方式: $PD=(V_{IN}-V_{OUT})\times I_{OUT}$

如: HT7550-2, SOT89 封装, 当 $V_{IN}=12V$, $I_{OUT}=100mA$ 时, 则 $PD=(12-5)\times 100mA=0.7W$, 超过规格的 0.5W, 可能会损坏 IC。不同封装的 PD 值, 请参考“热能信息”一栏。

典型应用电路



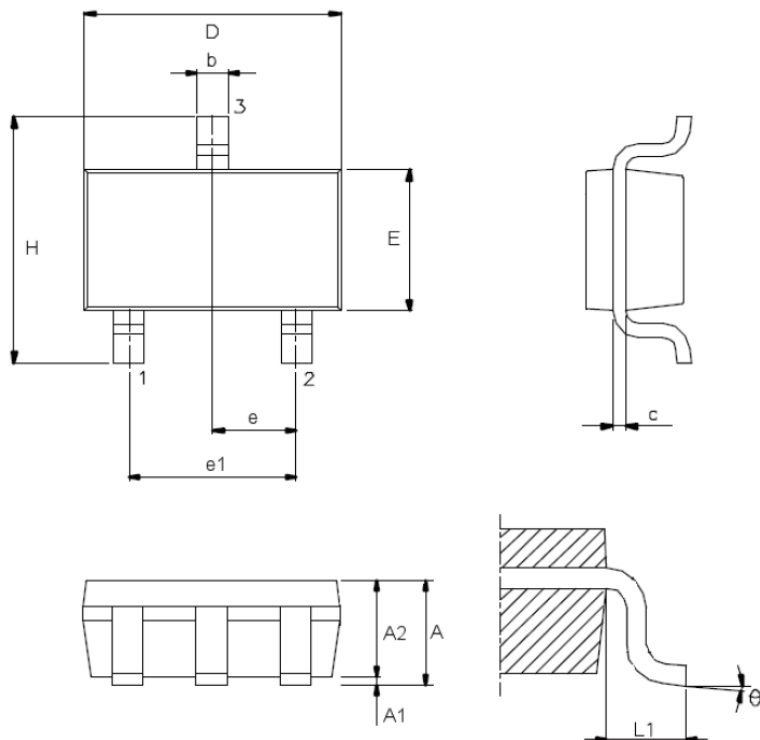
Layout 建议:

- 1、输入输出电容尽可能的靠近器件。
- 2、使用铜平面进行设备连接以优化热性能。
- 3、在器件周围仿真热通孔以分散热量。



封装信息

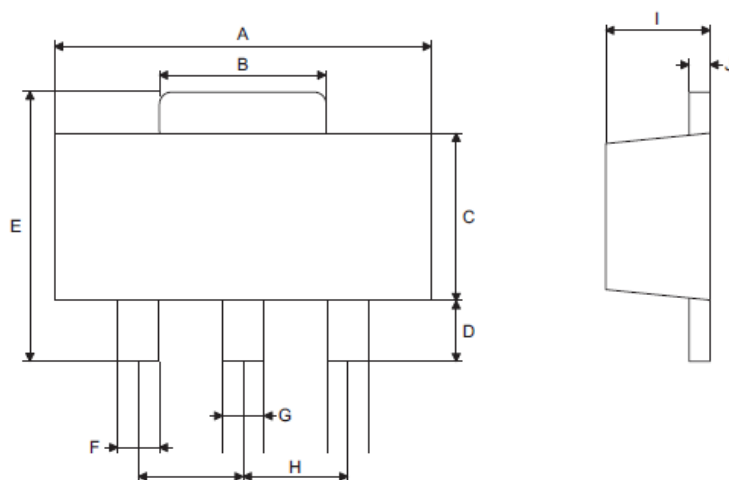
SOT-23-3L 封装尺寸



符号	尺寸 (单位: mm)		
	最小	典型	最大
A	—	—	1.45
A1	—	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
C	0.08	—	0.22
D	—	2.90	—
E	—	1.60	—
e	—	0.95	—
e1	—	1.90	—
H	—	2.80	—
L1	—	0.60	—
θ	0°	—	9°



SOT-89 封装尺寸



符号	尺寸（单位：mm）		
	最小	典型	最大
A	4.40	—	4.60
B	1.35	—	1.83
C	2.29	—	2.60
D	0.89	—	1.20
E	3.94	—	4.25
F	0.36	—	0.48
G	0.44	—	0.56
H	—	1.50	—
I	1.40	—	1.60
J	0.35	—	0.44



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